Virtium
Solid State Storage and Memory

DDR Memory Technology Comparison

DRAM Technology Comparison	SDR DRAM	DDR SDRAM	DDR2 SDRAM	DDR3 SDRAM	DDR4 SDRAM
		PC-1600	PC2-3200	PC3-6400	PC4-2133
	528				
Module Bandwidth (MB/s)		PC-2100	PC2-4200	PC3-8500	PC4-2400
	800				
Module speed bin, 64bit data bus		PC-2700	PC2-5300	PC3-10600	PC4-2666
	1064				
		PC-3200	PC2-6400	PC3-12800	PC4-3200
		DDR-200	DDR2-400	DDR3-800	DDR4-2133
	PC66				
Data rate (Mb/s per pin),		DDR-266	DDR2-533	DDR3-1066	DDR4-2400
	PC100				
Chip speed bin *(*Note 3)*		DDR-333	DDR2-667	DDR3-1333	DDR4-2666
	PC133				
		DDR-400	DDR2-800	DDR3-1600	DDR4-3200
		100	200	400	
	66				1067
		133	266	533	
Clock (Mhz)	100				1200
		166	333	666	
	133				1600
		200	400	800	
Module ranks					
	1, 2	1, 2, 4	1, 2, 4	1, 2, 4	1, 2, 4
(# of chip select lines)					
Module data bus width	x64,	x16, x32, x64,	x16, x32, x64,	x16, x32, x64,	x16, x32, x64
(I/O organization)	(x72 with ECC)	(x72 with ECC)	(x72 with ECC)	(x72 with ECC)	(x72 with ECC)
			VLP	VLP	VLP
	RDIMM	RDIMM	RDIMM	RDIMM	RDIMM
	UDIMM	UDIMM	UDIMM	UDIMM	UDIMM
	SODIMM	SODIMM	SODIMM	SODIMM	SODIMM
			SO-CDIMM	SO-UDIMM	SODIMM ECC
JEDEC Modules and			SO-RDIMM	SO-RDIMM	Reg SODIMM ECC
		microDIMM	microDIMM	microDIMM	
JEDEC Form Factors			mini-DIMM	mini-DIMM	mini-DIMM
			FB-DIMM	LR-DIMM	LR-DIMM
		16b-SODIMM	16b-SODIMM		
			32b-SODIMM	32b-SODIMM	
		32b-DIMM			
			SODIMM	SODIMM	
Module Thermal Sensor					All
			FB-DIMM	LR-DIMM	
Module pin-out *(*Note 1)*			New	Same as DDR2	
Module Densities	up to 256MB	128MB to 2GB	256MB to 4GB	1GB to 32GB	4GB to 64GB
Chip Densities	32Mb to 256Mb	128Mb to 1Gb	256Mb to 2Gb	512Mb to 8Gb	4Gb to 8Gb
Chip Density @ Lowest Cost per Bit	128Mb	256Mb	512Mb	1Gb	4Gb
Chip data bus width					
	x4, x8, x16	x4, x8, x16	x4, x8, x16	x4, x8, x16	
(I/O organization)					
Voltage (VDD = VDDQ/[V])	3.3 (+/- 0.3)	2.5 (+/- 0.2)	1.8 (+/- 0.1)	1.5 (+/- 0.075)	1.25V

% Power Reduction from previous generation (VDD only) *(*Note 2)*		32% reduction	39% reduction	20% reduction	25% reduction
On-die Thermal Sensor (ODTS)				Each DRAM	Each DRAM
Interface	LVTTL	SSTL_2	SSTL_18	SSTL_15	
DRAM Banks (inside the chip)	2/4	4	4 (8 for 1Gb)	8	
Prefetch (bits)	1	2	4	8	
Burst length *(*Note 5)*	1, 2, 4, 8 (page)	2, 4, 8	4, 8	8 (4 burst chop)	
Bidirectional strobe	None	Single Ended (SE)	SE, Differential optional	Differential only	
DQ driver strength/calibration	Wide envelope	Narrow envelope	18 Ω ,OCD calibration	34 Ω , ZQ-pin self-calibration	
Termination		only on MoBo	MoBo/ODT values = 50, 75, 150, or “off””	DIMM/Dynamic ODT	
Read Latency *(*Note 3)*	CL = (1), 2, 3	CL = (1.5), 2, 2.5, (3)	CL = (2), 3, 4, 5	CL = 5, 6, 7, 8, 9, 10, (11)	
Read Additional Latency	–	–	AL = 0, 1, 2, 3, 4	AL = 0, CL-1, CL-2	
Write Latency	0	1	RL-1	5, 6, 7, 8 + AL	
Data mask	Yes	Yes	Yes	Yes	
Interrupts	Yes	Yes	Wr-Wr, Rd-Rd 4n only	Burst Chop for Rd and Wr	
DRAM Package (monolithic)	TSOP-54	TSOP-66, BGA	FBGA only	FBGA only	FBGA only
DRAM ballout (On-DIMM Mirror friendly)	No	No	No	Yes	
Asynchronous Master RESET pin	No	No	No	Yes. Interrupt reset for system flexibility.	
Support of system level flight time compensation	No	No	No	Yes	
DRAM CWL (programable CAS Write Latency) per speed bin *(*Note 6)*	No	No	No	Yes	
On-die IO calibration engine	No	No	No	Yes. (data auto-calibration on the output buffer for high speed interface operation through ZC)	
Fly-by CAC (command/address/control) bus with On-DIMM termination	No	No	No	Yes	
Read/Write Leveling	No	No	No	Yes	
Memory sockets per channel *(*Note 4)*	4	4	4	4/2	
High precision calibration resistors on the DIMM	No	No	No	Yes	

Notes:

1. DDR2 and DDR3 UDIMMs and RDIMMs have a 240-pin, 1.0mm pitch memory sockets.
2. DDR3 may be as much as 30% reduction over DDR2 at the same speed, when considering lower IDD currents and other DDR3 architectural changes. DDR3-1600 is at the same power level, as DDR2-800.
3. DDR3 has higher CAS Latency then DDR2: DDR3-800 (5-5-5), DDR3-1066 (7-7-7), DDR3-1333 (8-8-8), DDR3-1333 (9-9-9).
4. The memory sockets (slots) per channel is memory controller and motherboard dependent. RDIMMs may have more slots then UDIMM. Faster and higher density DIMMs may require less slots per channel.
5. “DDR3 Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]”.
6. DDR3 Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600).