

Product Specifications		
PART NO.:	VL51B2863A-F8M	REV: 1.1

General Information

1GB 128Mx72 DDR3 SDRAM ECC UNBUFFERED Mini-DIMM 244-PIN

Description

The VL51B2863A is a 128Mx72 DDR3 SDRAM high density Mini-DIMM. This memory module is single rank, consists of nine CMOS 128Mx8 bits with 8 banks DDR3 Synchronous DRAMs in BGA packages, and a 2K EEPROM in an 8-pin MLF package. This module is a 244-pin mini dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features

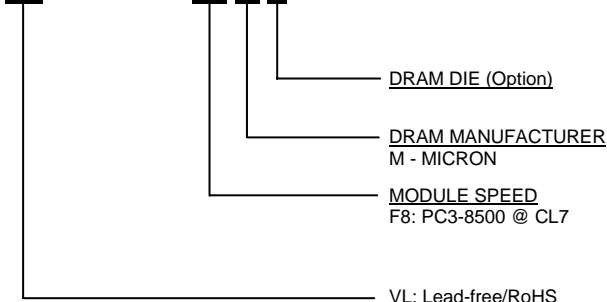
- 244-pin, mini dual in-line memory module (Mini-DIMM)
- Supports ECC error detection and correction
- Fast data transfer rate: maximum PC3-8500
- VDD = VDDQ = 1.5V +/-0.075V
- JEDEC standard 1.5V +/-0.075V I/O (SSTL_15)
- VDDSPD = 3.0V to 3.6V
- Eight internal component banks for concurrent operation
- 8-bit pre-fetch architecture
- Bi-directional differential data-strobe
- Nominal and dynamic on-die termination (ODT)
- ZQ calibration support
- Programmable CAS# latency: 7 (DDR3-1066)
- Programmable burst; length (8)
- Average refresh period 7.8 us
- Asynchronous reset
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 30mm (1.181"), double side components

Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Stobes
DQS0#~DQS8#	Data Stobes Complement
DM0~DM8	Data Masks
CB0~CB7	Data Check Bits I/O
CK0, CK0#	Clock Input
ODT0	On-die Termination Control
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Stobes
CAS#	Column Address Stobes
WE#	Write Enable
VDD	Voltage Supply 1.5V +/- 0.075V
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply 3.0V to 3.6V
VTT	Termination Voltage
RESET#	Register and SDRAM Control
NC	No Connect

Order Information:

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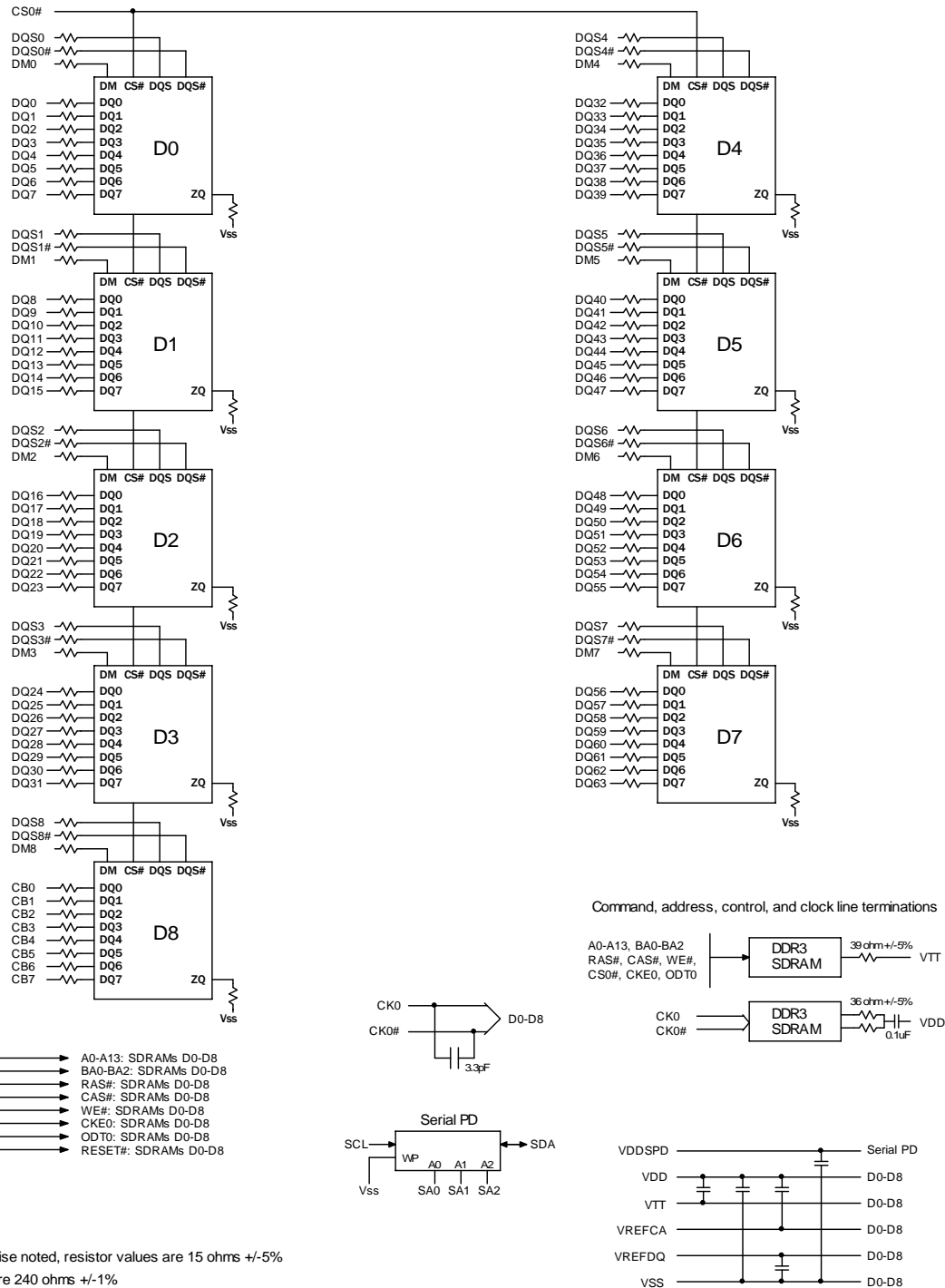
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Pin Configuration

244-PIN DDR3 Mini-DIMM FRONT SIDE								244-PIN DDR3 Mini-DIMM BACK SIDE							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VTT	31	DQ24	62	A2	92	DQ40	123	VTT	153	DQ29	184	A1	214	DQ45
2	VREFDQ	32	DQ25	63	VDD	93	DQ41	124	VSS	154	VSS	185	VDD	215	VSS
3	VSS	33	VSS	64	CK1 *	94	VSS	125	DQ4	155	DM3	186	CK0	216	DM5
4	DQ0	34	DQS3#	65	CK1# *	95	DQS5#	126	DQ5	156	NC	187	CK0#	217	NC
5	DQ1	35	DQS3	KEY		96	DQS5	127	VSS	157	VSS	KEY		218	VSS
6	VSS	36	VSS	66	VDD	97	VSS	128	DM0	158	DQ30	188	VDD	219	DQ46
7	DQS0#	37	DQ26	67	VREFCA	98	DQ42	129	NC	159	DQ31	189	VDD	220	DQ47
8	DQS0	38	DQ27	68	VDD	99	DQ43	130	VSS	160	VSS	190	EVENT# *	221	VSS
9	VSS	39	VSS	69	PAR_IN *	100	VSS	131	DQ6	161	CB4	191	A0	222	DQ52
10	DQ2	40	CB0	70	VDD	101	DQ48	132	DQ7	162	CB5	192	VDD	223	DQ53
11	DQ3	41	CB1	71	A10/ AP	102	DQ49	133	VSS	163	VSS	193	BA1	224	VSS
12	VSS	42	VSS	72	BA0	103	VSS	134	DQ12	164	DM8	194	VDD	225	DM6
13	DQ8	43	DQS8#	73	VDD	104	DQS6#	135	DQ13	165	NC	195	RAS#	226	NC
14	DQ9	44	DQS8	74	WE#	105	DQS6	136	VSS	166	VSS	196	CS0#	227	VSS
15	VSS	45	VSS	75	CAS#	106	VSS	137	DM1	167	CB6	197	VDD	228	DQ54
16	DQS1#	46	CB2	76	VDD	107	DQ50	138	NC	168	CB7	198	ODT0	229	DQ55
17	DQS1	47	CB3	77	CS1# *	108	DQ51	139	VSS	169	VSS	199	A13	230	VSS
18	VSS	48	VSS	78	ODT1 *	109	VSS	140	DQ14	170	NC	200	VDD	231	DQ60
19	DQ10	49	NC	79	VDD	110	DQ56	141	DQ15	171	TEST *	201	CS3# *	232	DQ61
20	DQ11	50	RESET#	80	CS2# *	111	DQ57	142	VSS	172	CKE1 *	202	NC	233	VSS
21	VSS	51	CKE0	81	NC	112	VSS	143	DQ20	173	VDD	203	VSS	234	DM7
22	DQ16	52	VDD	82	VSS	113	DQS7#	144	DQ21	174	A15 *	204	DQ36	235	NC
23	DQ17	53	BA2	83	DQ32	114	DQS7	145	VSS	175	A14 *	205	DQ37	236	VSS
24	VSS	54	ErrOut# *	84	DQ33	115	VSS	146	DM2	176	VDD	206	VSS	237	DQ62
25	DQS2#	55	VDD	85	VSS	116	DQ58	147	NC	177	A12/ BC#	207	DM4	238	DQ63
26	DQS2	56	A11	86	DQS4#	117	DQ59	148	VSS	178	A9	208	NC	239	VSS
27	VSS	57	A7	87	DQS4	118	VSS	149	DQ22	179	VDD	209	VSS	240	VDDSPD
28	DQ18	58	VDD	88	VSS	119	SA0	150	DQ23	180	A8	210	DQ38	241	SA1
29	DQ19	59	A5	89	DQ34	120	SCL	151	VSS	181	A6	211	DQ39	242	SDA
30	VSS	60	A4	90	DQ35	121	SA2	152	DQ28	182	VDD	212	VSS	243	VSS
		61	VDD	91	VSS	122	VTT			183	A3	213	DQ44	244	VTT

*: These pins are not used in this module.

Function Block Diagram



- A0-A13 → A0-A13: SDRAMs D0-D8
- BA0-BA2 → BA0-BA2: SDRAMs D0-D8
- RAS# → RAS#: SDRAMs D0-D8
- CAS# → CAS#: SDRAMs D0-D8
- WE# → WE#: SDRAMs D0-D8
- CKE0 → CKE0: SDRAMs D0-D8
- ODT0 → ODT0: SDRAMs D0-D8
- RESET# → RESET#: SDRAMs D0-D8

Notes:

1. Unless otherwise noted, resistor values are 15 ohms +/-5%
2. ZQ resistors are 240 ohms +/-1%

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Absolute Maximum Ratings					
Symbol	Parameter	MIN	MAX	Unit	
VDD	Voltage on VDD pin relative to VSS	-0.4	1.975	V	
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4	1.975	V	
VIN, VOUT	Voltage on any pin relative to VSS	-0.4	1.975	V	
TSTG	Storage temperature	-55	150	°C	
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, BA	-18	18	uA
		CS#, CKE, ODT, CK, CK#	-18	18	uA
		DM	-2	2	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	-5	5	uA	
IVREF	VREF supply leakage current; VREF = Valid VREF level	-9	9	uA	

DC Operating Conditions						
Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	I/O Supply Voltage	1.425	1.5	1.575	V	1,2
VREFDQ (DC)	I/O reference voltage DQ bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VREFCA (DC)	Input reference voltage CMD/ADD bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VTT	Termination Reference Voltage	-0.483 x VDDQ	0.5 x VDDQ	+0.517 x VDDQ	V	5

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VDD
4. For reference: approximate VDD/2 +/-15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 95	°C	1,2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At 0 – 85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TOPER <= 95°C.

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Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
Command and Address				
VIHCA(DC)	Input High (Logic 1) Voltage	VREF + 0.100	VDD	V
VILCA(DC)	Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1) Voltage	VREF + 0.100	VDD	V
VILDQ(DC)	Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
Command and Address				
VIHCA(AC)	Input High (Logic 1) Voltage	VREF + 0.175	-	V
VILCA(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.175	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1) Voltage	VREF + 0.175	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.175	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	F8 (DDR3-1066)		Unit
		Min	Max	
Input capacitance (A0~A13, BA0~BA2,RAS#,CAS#,WE#)	CIN1	10.75	17.5	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	10.75	17.5	pF
Input capacitance (CK0, CK0#)	CIN3	11.2	18.4	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	5.5	7	pF

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IDD Specification

Condition	Symbol	F8 (DDR3-1066)	Unit
Operating one bank active-precharge current; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	900	mA
Operating one bank active-read-precharge current; IOU = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); tRCD= tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	1080	mA
Precharge power-down current; All device banks idle; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F**	225	mA
	IDD2P-S**	90	mA
Precharge standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N**	495	mA
Precharge quiet standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	450	mA
Active power-down current; All device banks open; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	270	mA
Active standby current; All device banks open; tCK= tCK(IDD); tRP= tRP(IDD); tRAS= tRAS MAX(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	495	mA
Operating burst read current; All device banks open; Continuous burst reads; IOU = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1440	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	1440	mA
Burst refresh current; tCK=tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	1980	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	63	mA
Operating bank interleave read current; All bank interleaving reads; IOU = 0mA; BL = 8; CL = CL(IDD); AL = tRCD(IDD) - 1*tCK(IDD); tCK= tCK(IDD); tRC= tRC(IDD); tRRD = tRRD(IDD); tRCD = 1*tCK(IDD); CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	3510	mA
Note: IDD specification is based on Micron F-die components. *: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode. **: Value calculated reflects all module ranks in this operating condition.			



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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	F8 (DDR3-1066)		Unit
		MIN	MAX	
Clock Timing				
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	1.875	<2.5	ns
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ns
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-90	90	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	160		ps
Cumulative error across 2 cycles	tERR(2per)	-132	132	ps
Cumulative error across 3 cycles	tERR(3per)	-157	157	ps
Cumulative error across 4 cycles	tERR(4per)	-175	175	ps
Cumulative error across 5 cycles	tERR(5per)	-188	188	ps
Cumulative error across 6 cycles	tERR(6per)	-200	200	ps
Cumulative error across 7 cycles	tERR(7per)	-209	209	ps
Cumulative error across 8 cycles	tERR(8per)	-217	217	ps
Cumulative error across 9 cycles	tERR(9per)	-224	224	ps
Cumulative error across 10 cycles	tERR(10per)	-231	231	ps
Cumulative error across 11 cycles	tERR(11per)	-237	237	ps
Cumulative error across 12 cycles	tERR(12per)	-242	242	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	$tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min$ $tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max$		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	150	ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-600	300	ps
DQ high-impedance time from CK, CK#	tHZ(DQ)	-	300	ps
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	tDS(base)	25	-	ps
Data hold time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	tDH(base)	100	-	ps
DQ and DM Input pulse width for each input	tDIPW	490	-	ps

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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	F8 (DDR3-1066)		Unit
		MIN	MAX	
Data Strobe Timing				
DQS, DQS# READ Preamble	tRPRE	0.9	-	tCK
DQS, DQS# differential READ Postamble	tRPST	0.3	-	tCK
DQS, DQS# output high time	tQSH	0.38	-	tCK(avg)
DQS, DQS# output low time	tQSL	0.38	-	tCK(avg)
DQS, DQS# WRITE Preamble	tWPRE	0.9	-	tCK
DQS, DQS# WRITE Postamble	tWPST	0.3	-	tCK
DQS, DQS# rising edge output access time from rising CK, CK#	tDQCK	-300	300	ps
DQS, DQS# low-impedance time (Referenced from RL-1)	tLZ(DQS)	-600	300	ps
DQS, DQS# high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	300	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	tCK(avg)
DQS, DQS# falling edge hold time to CK, CK# rising edge	tDSH	0.2	-	tCK(avg)
Command and Address Timing				
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK, 15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	37.5	9*tREFI	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK, 7.5ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK, 10ns)	-	
Four activate window for 1KB page size	tFAW	37.5	-	ns
Four activate window for 2KB page size	tFAW	50	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	125	-	ps
Command and Address hold time from CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIH(base)	200	-	ps
Control & Address Input pulse width for each input	tIPW	780	-	ps



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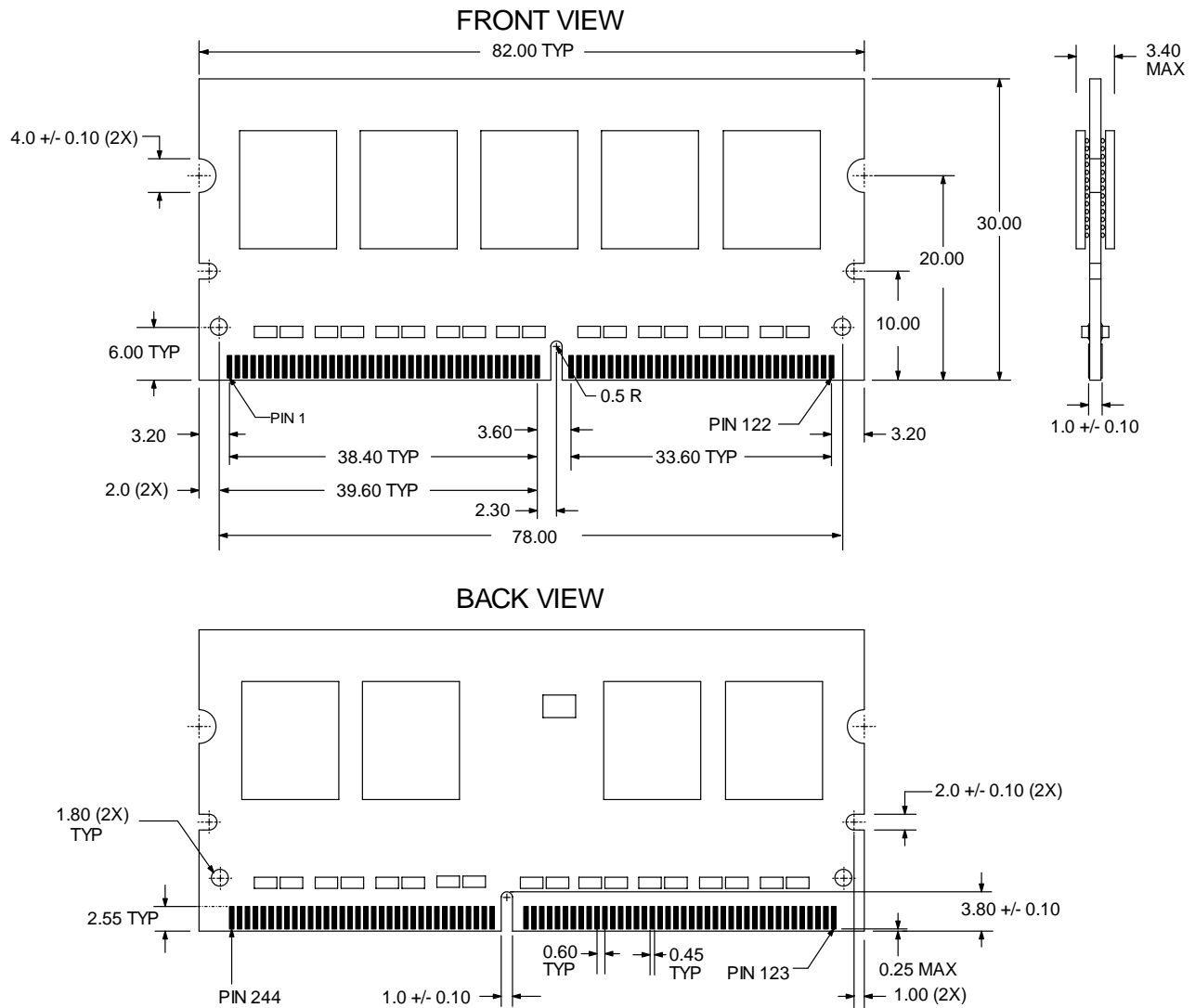
AC TIMING PARAMETERS & SPECIFICATIONS				
Parameter	Symbol	F8 (DDR3-1066)		Unit
		MIN	MAX	
Refresh Timing				
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	110	-	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8		us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9		us
Calibration Timing				
Power-up and RESET calibration time	tZQinitl	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation Short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC + 10ts)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	Max(5tCK, tRFC + 10ts)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	Max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	Max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max (3tCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	
Timing of WR command to Power Down entry BL8 (OTF, MRS), BL4OTF	tWRPDEN	WL + 4 + (tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry BL8 (OTF, MRS), BL4OTF	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 + (tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	

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		MIN	MAX	
ODT Timing				
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	ns
ODT turn-on	tAON	-300	300	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQSS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	245	-	ps
Hold time for tDQSS latch	tWLH	245	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

Product Specifications		
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Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.



Product Specifications		
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Revision History:

Date	Rev.	Page	Changes
08/13/2009	1.0	All	Spec release
11/08/2010	1.1	1, 5-11	Adding "single rank" on description page 1 Update package dimension drawing page 11 Changing the way module speed show on the spec page 5-10