



# Product Specifications

PART NO:

VL495T2953-E6S/D5S/CCS

REV: 1.3

## General Information

### 1GB 128Mx72 DDR2 SDRAM ECC REGISTERED Mini-DIMM 244-PIN

**Description:** The VL495T2953 is a 128Mx72 Double Data Rate DDR2 SDRAM high density Mini-DIMM. This memory module consists of eighteen CMOS 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, two 14-bit Registered buffers in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin TSSOP package. This module is a 244-pin mini dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

### Features:

- . 244-pin, mini dual in-line memory module (Mini-DIMM)
- . Fast data transfer rates: PC2-5300, PC2-4200, and PC2-3200
- . VDD = VDDQ = 1.8V
- . VDDSPD = 1.7V to 3.6V
- . JEDEC standard 1.8V I/O (SSTL\_18 compatible)
- . Differential data strobe (DQS, DQS#) option
- . Four-bit prefetch architecture
- . DLL aligns DQ and DQS transition with CK
- . Programmable CAS# Latency (CL): 3, 4 & 5
- . Programmable burst; length (4, 8)
- . On-die termination (ODT)
- . PCB Height: 1.181", double sided components

Pin Name	Function
A0-A13	Address Inputs
BA0-BA1	Bank Address Inputs
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data Stobes
DQS0#-DQS8#	Data Stobes Complement
ODT0,ODT1	On-die Termination Control
CK0,CK0#	Clock Input
CKE0,CKE1	Clock Enables
CS0#,CS1#	Chip Selects
RAS#	Row Address Stobes
CAS#	Column Address Stobes
WE#	Write Enable
RESET#	Register Reset Input
DM0-DM8	Data Masks
VDD	Voltage Supply 1.8V +/- 0.1V
A10/AP	Address Input/Auto Precharge
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VDDQ	I/O Power (1.8v)
VSS	Ground
SA0-SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VREF	SSTL_18 Reference Voltage
NC	No Connect

### Order Information:

**VL495T2953-E6 S X**

DRAM DIE (Option)

DRAM MANUFACTURER  
S - SAMSUNG

MODULE SPEED  
CC: PC2-3200 @ CL3  
D5: PC2-4200 @ CL4  
E6: PC2-5300 @ CL5

VL : Lead-free/RoHS



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## Pin Configuration

244-PIN DDR2 Mini-DIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	123	VSS	32	VSS	154	DQ28	63	VDDQ	185	A3	92	DQ41	214	VSS
2	VSS	124	DQ4	33	DQ24	155	DQ29	64	A2	186	A1	93	VSS	215	DM5
3	DQ0	125	DQ5	34	DQ25	156	VSS	65	VDD	187	VDD	94	DQS5#	216	NC
4	DQ1	126	VSS	35	VSS	157	DM3		KEY			95	DQS5	217	VSS
5	VSS	127	DM0	36	DQS3#	158	NC					96	VSS	218	DQ46
6	DQS0#	128	NC	37	DQS3	159	VSS	66	VSS	188	CK0	97	DQ42	219	DQ47
7	DQS0	129	VSS	38	VSS	160	DQ30	67	VSS	189	CK0#	98	DQ43	220	VSS
8	VSS	130	DQ6	39	DQ26	161	DQ31	68	NC	190	VDD	99	VSS	221	DQ52
9	DQ2	131	DQ7	40	DQ27	162	VSS	69	VDD	191	A0	100	DQ48	222	DQ53
10	DQ3	132	VSS	41	VSS	163	CB4	70	A10/AP	192	BA1	101	DQ49	223	VSS
11	VSS	133	DQ12	42	CB0	164	CB5	71	BA0	193	VDD	102	VSS	224	NC
12	DQ8	134	DQ13	43	CB1	165	VSS	72	VDD	194	RAS#	103	SA2	225	NC
13	DQ9	135	VSS	44	VSS	166	DM8	73	WE#	195	VDDQ	104	NC	226	VSS
14	VSS	136	DM1	45	DQS8#	167	NC	74	VDDQ	196	CS0#	105	VSS	227	DM6
15	DQS1#	137	NC	46	DQS8	168	VSS	75	CAS#	197	VDDQ	106	DQS6#	228	NC
16	DQS1	138	VSS	47	VSS	169	CB6	76	VDDQ	198	ODT0	107	DQS6	229	VSS
17	VSS	139	NC	48	CB2	170	CB7	77	CS1#	199	A13	108	VSS	230	DQ54
18	RESET#	140	NC	49	CB3	171	VSS	78	ODT1	200	VDD	109	DQ50	231	DQ55
19	NC	141	VSS	50	VSS	172	NC	79	VDDQ	201	NC	110	DQ51	232	VSS
20	VSS	142	DQ14	51	NC	173	VDDQ	80	NC	202	VSS	111	VSS	233	DQ60
21	DQ10	143	DQ15	52	VDDQ	174	CKE1	81	VSS	203	DQ36	112	DQ56	234	DQ61
22	DQ11	144	VSS	53	CKE0	175	VDD	82	DQ32	204	DQ37	113	DQ57	235	VSS
23	VSS	145	DQ20	54	VDD	176	NC	83	DQ33	205	VSS	114	VSS	236	DM7
24	DQ16	146	DQ21	55	BA2*	177	NC	84	VSS	206	DM4	115	DQS7#	237	NC
25	DQ17	147	VSS	56	NC	178	VDDQ	85	DQS4#	207	NC	116	DQS7	238	VSS
26	VSS	148	DM2	57	VDDQ	179	A12	86	DQS4	208	VSS	117	VSS	239	DQ62
27	DQS2#	149	NC	58	A11	180	A9	87	VSS	209	DQ38	118	DQ58	240	DQ63
28	DQS2	150	VSS	59	A7	181	VDD	88	DQ34	210	DQ39	119	DQ59	241	VSS
29	VSS	151	DQ22	60	VDD	182	A8	89	DQ35	211	VSS	120	VSS	242	SDA
30	DQ18	152	DQ23	61	A5	183	A6	90	VSS	212	DQ44	121	SA0	243	SCL
31	DQ19	153	VSS	62	A4	184	VDDQ	91	DQ40	213	DQ45	122	SA1	244	VDDSPD

NC : No connection

RESET# (Pin 18) is connected to both OE of the PLL and RESET# of the register

\* : These pins are not used in this module.



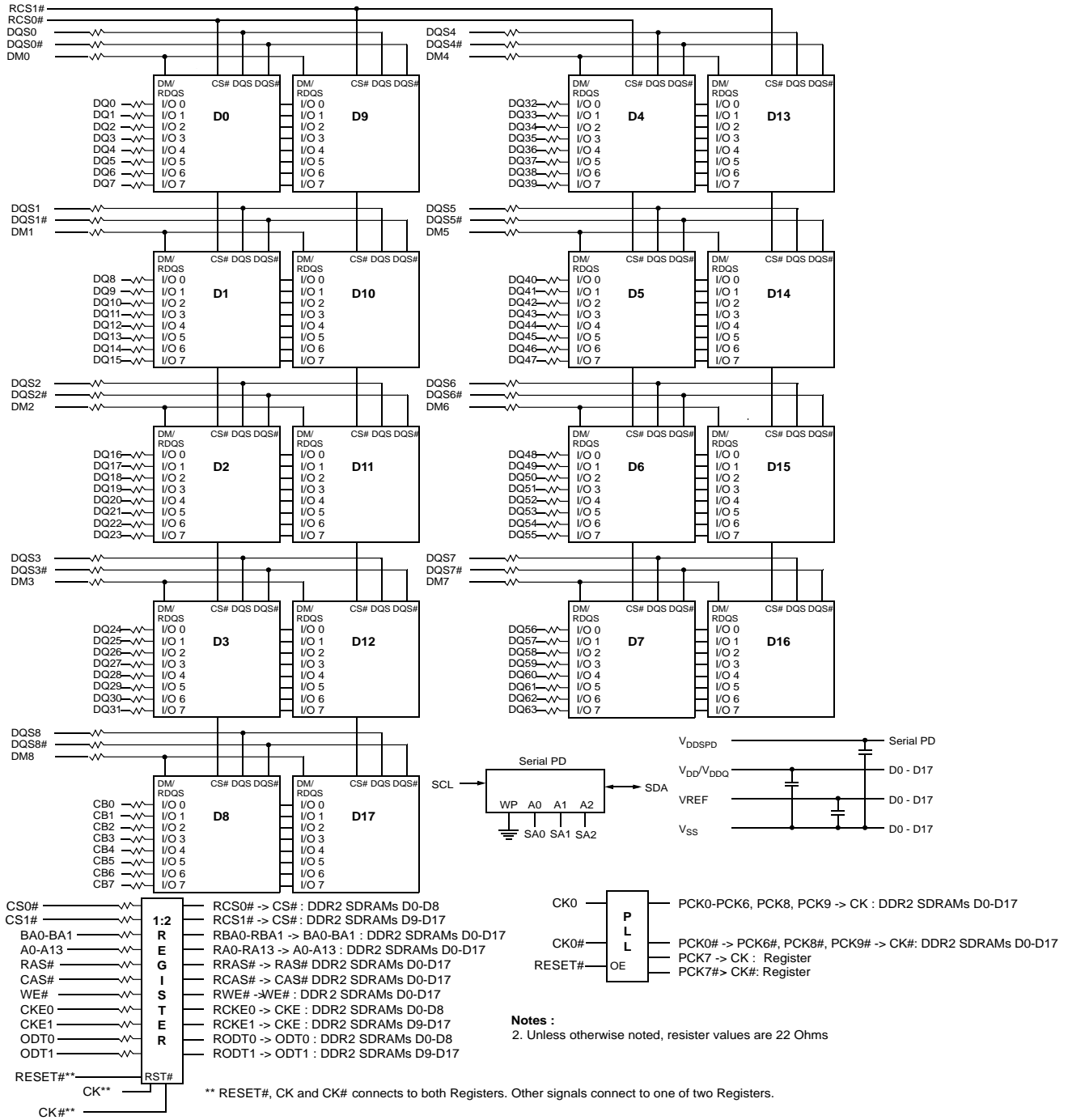
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## Functional Block Diagram





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## Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit	
V <sub>DD</sub>	Voltage on V <sub>DD</sub> pin relative to V <sub>SS</sub>	-1.0	2.3	V	
V <sub>DDQ</sub>	Voltage on V <sub>DDQ</sub> pin relative to V <sub>SS</sub>	-0.5	2.3	V	
V <sub>DDL</sub>	Voltage on V <sub>DDL</sub> pin relative to V <sub>SS</sub>	-0.5	2.3	V	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5	2.3	V	
T <sub>STG</sub>	Storage temperature	-55	100	°C	
T <sub>CASE</sub>	Device operating temperature	0	85	°C	
I <sub>L</sub>	Input leakage current; Any input 0V<V <sub>IN</sub> <V <sub>DD</sub> ; VREF input 0V<V <sub>IN</sub> <0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE, BA	-10	10	uA
		CK, CK#	-10	10	uA
		DM	-10	10	uA
I <sub>oz</sub>	Output leakage current; 0V<V <sub>OUT</sub> <V <sub>DDQ</sub> ; DQs and ODT are disabled	-10	10	uA	
I <sub>VREF</sub>	VREF leakage current; VREF = Valid VREF level	-36	36	uA	

## DC Operating Conditions

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V <sub>DD</sub>	1.7	1.8	1.9	V	1
I/O Supply voltage	V <sub>DDQ</sub>	1.7	1.8	1.9	V	4
VDDL Supply voltage	V <sub>DDL</sub>	1.7	1.8	1.9	V	4
I/O Reference voltage	V <sub>REF</sub>	0.49 x V <sub>DDQ</sub>	0.50 x V <sub>DDQ</sub>	0.51 x V <sub>DDQ</sub>	V	2
I/O Termination voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V	3

- Notes:
1. V<sub>DD</sub> V<sub>DDQ</sub> must track each other. V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
  2. V<sub>REF</sub> is expected to equal V<sub>DDQ</sub>/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on V<sub>REF</sub> may not exceed +/-2 percent of V<sub>REF</sub>. This measurement is to be taken at the nearest V<sub>REF</sub> bypass capacitor.
  3. V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.
  4. V<sub>DDQ</sub> tracks with V<sub>DD</sub>; V<sub>DDL</sub> tracks with V<sub>DD</sub>.



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VL495T2953-E6S/D5S/CCS

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## Operating Temperature Condition

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0 to 85	°C	V

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
2. At 0 - 85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TC <= 95°C

## Input DC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V <sub>IH</sub> (DC)	VREF + 0.125	VREF + 0.300	V
Input Low (Logic 0) Voltage	V <sub>IL</sub> (DC)	-0.300	VREF - 0.125	V

## Input AC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V <sub>IH</sub> (AC)	VREF + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V <sub>IH</sub> (AC)	VREF + 0.200	-	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V <sub>IL</sub> (AC)	-	VREF - 0.250	V
AC Input Low (Logic 0) Voltage DDR2-677	V <sub>IL</sub> (AC)	-	VREF - 0.200	V

## Input/Output Capacitance

T<sub>A</sub>=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA1,RAS#,CAS#,WE#)	CIN1	-	11	pF
Input capacitance (CKE0,CKE1), (ODT0,ODT1)	CIN2	-	11	pF
Input capacitance (CS0#,CS1#)	CIN3	-	11	pF
Input capacitance (CK0,CK0#)	CIN4	-	11	pF
Input capacitance (DM0 ~ DM8), (CB0 ~ CB7)	CIN5 (E6)	9	11	pF
	CIN5 (D5,CC)	9	12	pF
Input capacitance (DQ0 ~ DQ63), (DQS0 ~ DQS8)	COU1 (E6)	9	11	pF
	COU1 (D5,CC)	9	12	pF



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## IDD Specification

Condition	Symbol	-E6	-D5	-CC	Unit
<b>Operating one bank active-precharge;</b> $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS MIN(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	1337	1292	1292	mA
<b>Operating one bank active-read-precharge;</b> IOUT = 0mA; BL = 4; CL = CL(IDD); $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS MIN(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	1472	1427	1427	mA
<b>Precharge power-down current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P**	644	644	644	mA
<b>Precharge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	1130	1040	1040	mA
<b>Precharge standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	IDD2N**	1220	1130	1130	mA
<b>Active power-down current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0mA	1040	1040	1040	mA
		Slow PDN Exit MRS(12) = 1mA	716	716	716
<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS MIN(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	1490	1400	1400	mA
<b>Operating burst write current;</b> All banks open; Continuous burst writes; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	1832	1652	1562	mA
<b>Operating burst read current;</b> All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1877	1697	1562	mA
<b>Burst auto refresh current;</b> $t_{CK} = t_{CK(IDD)}$ ; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	3200	3020	3020	mA
<b>Self refresh current;</b> CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal IDD6**	144	144	144	mA
<b>Operating bank interleave read current;</b> All bank interleaving reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$ ; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; $t_{RCD} = 1 * t_{CK(IDD)}$ ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7*	2552	2552	2552	mA
Notes: IDDs were calculated using Samsung components. Other manufacturers' DRAMs may have different values. *: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode. **: Value calculated reflects all module ranks in this operating condition.					



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## AC Timing Parameters & Specifications

Parameter	Symbol	-E6		-D5		-CC		Unit		
		Min	Max	Min	Max	Min	Max			
Clock	Clock cycle time	CL=5	$t_{CK}(5)$	3000	8000	-	-	-	-	ps
		CL=4	$t_{CK}(4)$	3750	8000	3,750	8,000	5,000	8,000	ps
		CL=3	$t_{CK}(3)$	5000	8000	5,000	8,000	5,000	8,000	ps
	CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	
	CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	
	Half clock period	$t_{HP}$	MIN ( $t_{CH}, t_{CL}$ )		MIN ( $t_{CH}, t_{CL}$ )		MIN ( $t_{CH}, t_{CL}$ )			ps
	Clock jitter	$t_{JIT}$	-125	125	-125	125	-125	125		ps
Data	DQ output access time from CK/CK#	$t_{AC}$	-450	+450	-500	+500	-600	+600		ps
	Data-out high impedance window from CK/CK#	$t_{HZ}$		$t_{AC}(MAX)$		$t_{AC}(MAX)$		$t_{AC}(MAX)$		ps
	Data-out low-impedance window from CK/CK#	$t_{LZ}$	$t_{AC}(MIN)$	$t_{AC}(MAX)$	$t_{AC}(MIN)$	$t_{AC}(MAX)$	$t_{AC}(MIN)$	$t_{AC}(MAX)$		ps
	DQ and DM input setup time relative to DQS	$t_{DS}$	100		100		150			
	DQ and DM input hold time relative to DQS	$t_{DH}$	225		225		275			
	DQ and DM input pulse width (for each input)	$t_{DIPW}$	0.35		0.35		0.35			$t_{CK}$
	Data hold skew factor	$t_{OHS}$		340		400		450		ps
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access	$t_{QH}$	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$			ps
	Data valid output window (DVW)	$t_{DVW}$	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$			ns
Data Strobe	DQS input high pulse width	$t_{DQSH}$	0.35		0.35		0.35			$t_{CK}$
	DQS input low pulse width	$t_{DQSL}$	0.35		0.35		0.35			$t_{CK}$
	DQS output access time from CK/CK#	$t_{DQSOCK}$	-400	+400	-450	+450	-500	+500		ps
	DQS falling edge to CK rising – setup time	$t_{DSS}$	0.2		0.2		0.2			$t_{CK}$
	DQS falling edge from CK rising – hold time	$t_{DSH}$	0.2		0.2		0.2			$t_{CK}$
	DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$		240		300		350		ps
	DQS read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	0.9	1.1		$t_{CK}$
	DQS read postamble	$t_{RPST}$	0.4	0.6	0.4	0.6	0.4	0.6		$t_{CK}$
	DQS write preamble setup time	$t_{WPRES}$	0		0		0			ps
	DQS write preamble	$t_{WPRE}$	0.35		0.35		0.35			$t_{CK}$
	DQS write postamble	$t_{WPST}$	0.4	0.6	0.4	0.6	0.4	0.6		$t_{CK}$
	Write command to first DQS latching transition	$t_{DQSS}$	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25		$t_{CK}$



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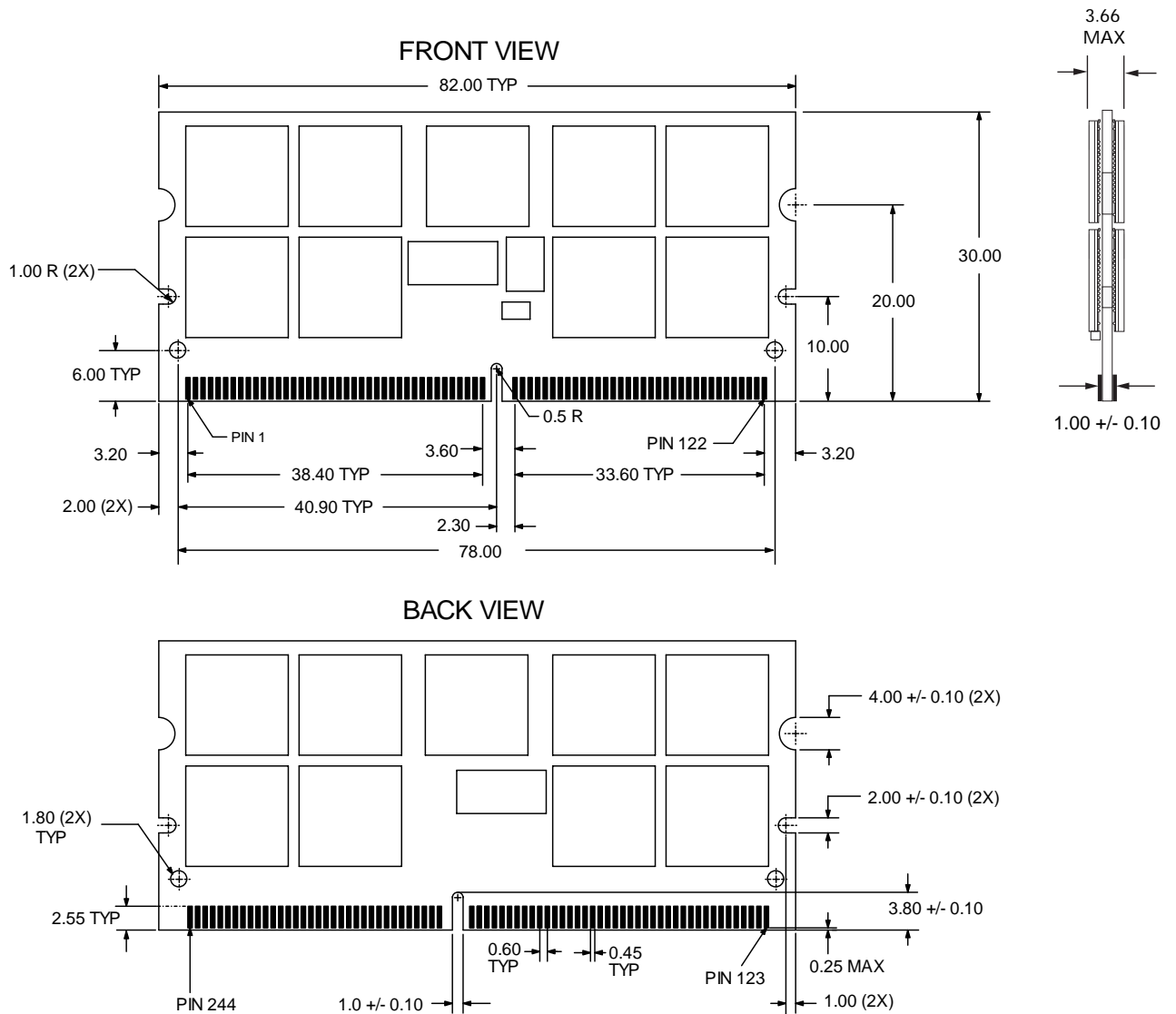
REV: 1.3

## AC Timing Parameters & Specifications ( cont' )

Parameter	Symbol	-E6		-D5		-CC		Unit	
		Min	Max	Min	Max	Min	Max		
Command and Address	Address and control input pulse width for each input	$t_{PW}$	0.6		0.6		0.6		$t_{CK}$
	Address and control input setup time	$t_{IS}$	200		250		250		ps
	Address and control input hold time	$t_{IH}$	275		375		475		ps
	CAS# to CAS# command delay	$t_{CCD}$	2		2		2		ps
	ACTIVE to ACTIVE (same bank) command	$t_{RC}$	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	$t_{RCD}$	15		15		15		ns
	Four Bank Activate period	$t_{FAW}$	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	$t_{RAS}$	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	$t_{RTP}$	7.5		7.5		7.5		ns
	Write recovery time	$t_{WR}$	15		15		15		ns
	Auto precharge write recovery + precharge time	$t_{DAL}$	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	$t_{WTR}$	10		7.5		10		ns
	PRECHARGE command period	$t_{RP}$	15		15		15		ns
	PRECHARGE ALL command period	$t_{RPA}$	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
	LOAD MODE command cycle time	$t_{MRD}$	2		2		2		$t_{CK}$
	CKE low to CK,CK# uncertainty	$t_{DELAY}$	4,375		4,375		4,375		ns
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	$t_{RFC}$	105	70,000	105	70,000	105	70,000	ns
	Average periodic refresh interval	$t_{REFI}$		7.8		7.8		7.8	us
	Exit self refresh to non-READ command	$t_{XSNR}$	$t_{RFC(MIN)} + 10$		$t_{RFC(MIN)} + 10$		$t_{RFC(MIN)} + 10$		ns
	Exit self refresh to READ	$t_{XSRD}$	200		200		200		$t_{CK}$
	Exit self refresh timing reference	$t_{ISXR}$	$t_{IS}$		$t_{IS}$		$t_{IS}$		ps
ODT	ODT turn-on delay	$t_{AOND}$	2	2	2	2	2	2	$t_{CK}$
	ODT turn-on	$t_{AON}$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	ps
	ODT turn-off delay	$t_{AOFD}$	2.5	2.5	2.5	2.5	2.5	2.5	$t_{CK}$
	ODT turn-off	$t_{AOF}$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	ps
	ODT turn-on (power-down mode)	$t_{AONPD}$	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	ps
	ODT turn-off (power-down mode)	$t_{AOFPD}$	$t_{AC(MIN)} + 2000$	$2.5 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2.5 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2.5 \times t_{CK} + t_{AC(MAX)} + 1000$	ps
	ODT to power-down entry latency	$t_{ANPD}$	3		3		3		$t_{CK}$
	ODT power-down exit latency	$t_{AXPD}$	8		8		8		$t_{CK}$
Power-Down	Exit active power-down to READ command, MR[bit12=0]	$t_{XARD}$	2		2		2		$t_{CK}$
	Exit active power-down to READ command, MR[bit12=1]	$t_{XARDS}$	7-AL		6-AL		6-AL		$t_{CK}$
	Exit precharge power-down to any non-READ command.	$t_{XP}$	2		2		2		$t_{CK}$
	CKE minimum high/low time	$t_{CKE}$	3		3		3		$t_{CK}$

<h1>Product Specifications</h1>		
PART NO:	VL495T2953-E6S/D5S/CCS	REV: 1.3

## Package Dimensions



**NOTE:**

All dimensions are in millimeters with tolerance +/-0.15mm unless otherwise specified.



## Product Specifications

PART NO:

VL495T2953-E6S/D5S/CCS

REV: 1.3

### Revision History:

Date	Rev.	Page	Changes
02/14/06	1.0	All	Spec release
03/15/07	1.1	6	IDD table update
03/25/09	1.2	1	Order Information update
08/31/10	1.3	All	Update datasheet