

Product Specifications		
PART NO.:	VL493T5663C-E6M/D5M/CCM	REV: 1.3

General Information

2GB 256Mx72 DDR2 SDRAM ECC REGISTERED SO-RDIMM 200-PIN

Description

The VL493T5663C is a 256Mx72 DDR2 SDRAM high density SO-RDIMM. This memory module is dual rank, consists of eighteen CMOS 128Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, two 25-bit registered buffer in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin MLF package. This module is a 200-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

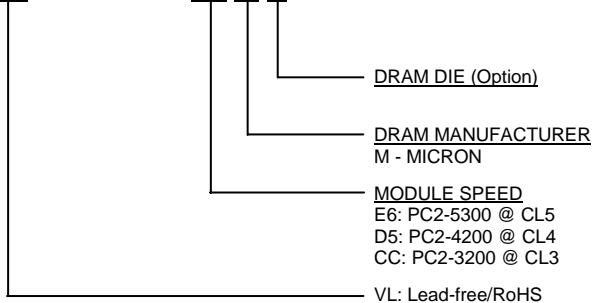
- 200-pin, registered small-outline dual in-line memory module (SO-RDIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rates: PC2-5300, PC2-4200, PC2-3200
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 5 (DDR2-667), 4 (DDR2-533), 3 (DDR2-400)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 29.85mm (1.175"), double sided component
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Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK, CK#	Clock Input
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
CB0~CB7	Check Bits
DM0~DM8	Data Masks
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

Order Information:

VL493T5663C-E6 M X





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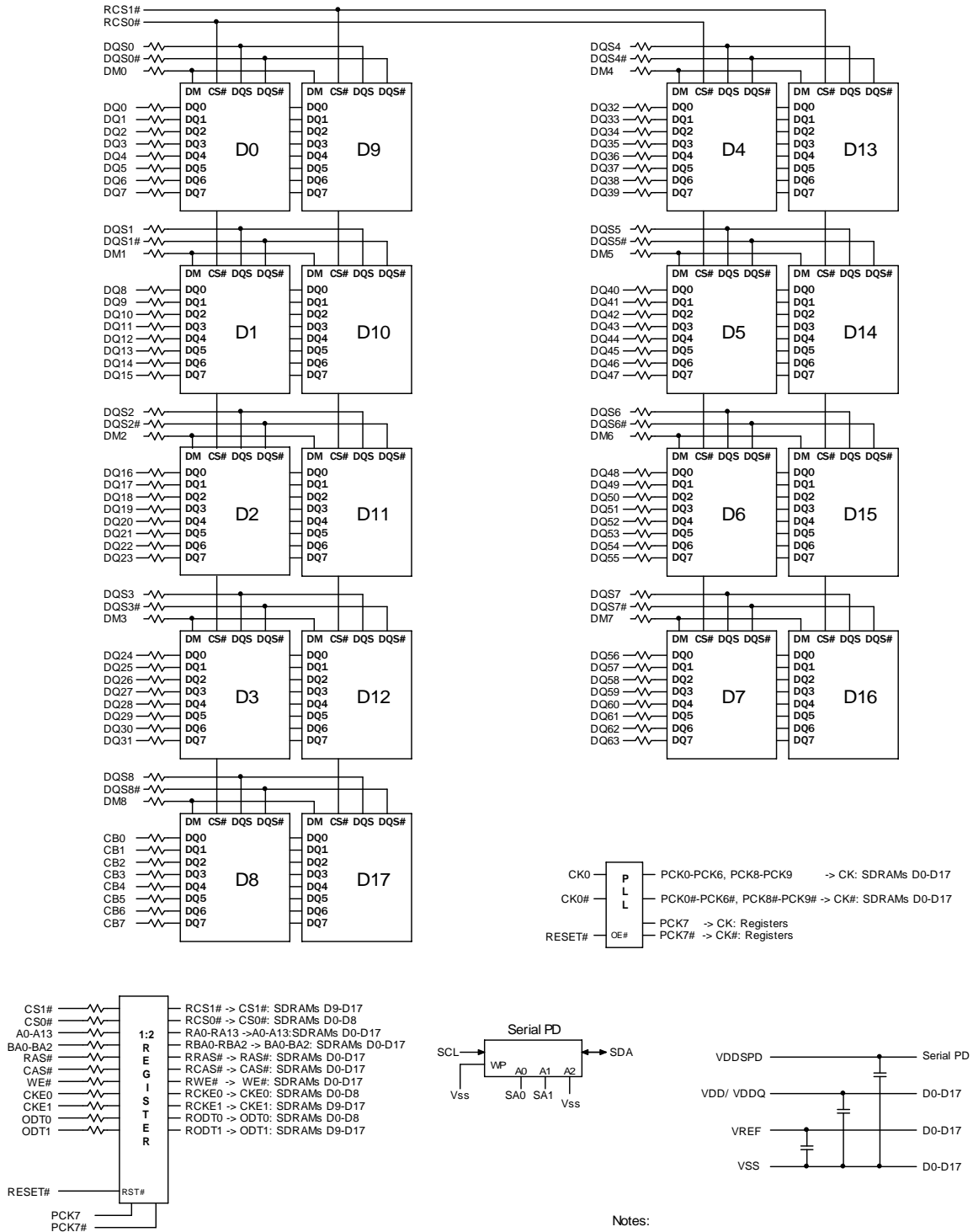
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Pin Configuration

200-PIN DDR2 SO-RDIMM FRONT								200-PIN DDR2 SO-RDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	51	DQ18	101	VDD	151	VSS	2	VSS	52	VSS	102	A6	152	VSS
3	DQ0	53	DQ19	103	A5	153	DQS5#	4	DQ4	54	DQ28	104	A4	154	DM5
5	VSS	55	VSS	105	A3	155	DQS5	6	DQ5	56	DQ29	106	VDD	156	VSS
7	DQ1	57	DQ24	107	A2	157	VSS	8	VSS	58	VSS	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	VDD	159	DQ42	10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	VSS	111	A10/AP	161	DQ43	12	VSS	62	VSS	112	BA1	162	VSS
13	VSS	63	DQS3#	113	BA0	163	VSS	14	DQ6	64	DQ30	114	VDD	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48	16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	VSS	117	VDD	167	DQ49	18	VSS	68	VSS	118	CS0#	168	VSS
19	VSS	69	DQ26	119	CAS#	169	VSS	20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	CS1#	171	DQS6#	22	DQ13	72	CB5	122	A13	172	VSS
23	DQ9	73	VSS	123	VDD	173	DQS6	24	VSS	74	VSS	124	VDD	174	DQ54
25	VSS	75	CB0	125	ODT1	175	VSS	26	DM1	76	DM8	126	CK	176	DQ55
27	DQS1#	77	CB1	127	NC	177	DQ50	28	VSS	78	VSS	128	CK#	178	VSS
29	DQS1	79	VSS	129	DQ32	179	DQ51	30	DQ14	80	CB6	130	VSS	180	DQ60
31	VSS	81	DQS8#	131	VSS	181	VSS	32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56	34	VSS	84	VSS	134	DQ37	184	VSS
35	DQ11	85	VSS	135	DQS4#	185	DQ57	36	DQ20	86	CB2	136	VSS	186	DM7
37	VSS	87	CKE0	137	DQS4	187	VSS	38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	CKE1	139	VSS	189	DQS7#	40	VSS	90	VSS	140	VSS	190	VSS
41	DQ17	91	NC	141	DQ34	191	DQS7	42	RESET#	92	BA2	142	DQ38	192	DQ63
43	VSS	93	VDD	143	DQ35	193	DQ58	44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	VSS	195	VSS	46	VSS	96	A11	146	VSS	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59	48	DQ22	98	VDD	148	DQ44	198	SA1
49	VSS	99	A7	149	DQ41	199	VDDSPD	50	DQ23	100	A8	150	DQ45	200	SA0

Note: NC: No connect

Function Block Diagram



Notes:

1. Unless otherwise noted, resistor values are 22 ohms +/-5%

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Absolute Maximum Ratings					
Symbol	Parameter	MIN	MAX	Unit	
VDD	Voltage on VDD pin relative to VSS	-1.0	2.3	V	
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5	2.3	V	
VDDL	Voltage on VDDL pin relative to VSS	-0.5	2.3		
VIN, VOUT	Voltage on any pin relative to VSS	-0.5	2.3	V	
TSTG	Storage temperature	-55	150	°C	
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-10	10	uA
		CS#, CKE, ODT	-10	10	uA
		CK, CK#	-250	+250	uA
		DM	-10	10	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	-10	10	uA	
IVREF	VREF supply leakage current; VREF = Valid VREF level	-36	36	uA	

DC Operating Conditions						
Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3
<p>Note:</p> <ol style="list-style-type: none"> 1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD. 2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor. 3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF. 4. VDDQ tracks with VDD; VDDL tracks with VDD. 						



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Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 85	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 - 85°C, operation temperature range, all DRAM specifications will be supported.				

Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage DDR2-400 & DDR2-533	VREF + 0.250	-	V
VIH(AC)	Input High (Logic 1) Voltage DDR2-667	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	-	VREF - 0.250	V
VIL(AC)	Input Low (Logic 0) Voltage DDR2-667	-	VREF - 0.200	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	9	11	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT), (CS0#, CS1#)	CIN2	9	11	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	9	12	pF

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IDD Specification

Condition	Symbol	E6 (DDR2-667)	D5 (DDR2-533)	CC (DDR2-400)	Unit	
Operating one bank active-pre-charge current; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	1228	1093	1093	mA	
Operating one bank active-read-pre-charge current; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1*	1363	1318	1273	mA	
Pre-charge power-down current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P**	526	526	526	mA	
Pre-charge quiet standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	1120	1120	1030	mA	
Pre-charge standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	IDD2N**	1120	1120	1030	mA	
Active power-down current; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	940	940	940	mA	
	Slow PDN Exit MRS(12) = 1	580	580	580	mA	
Active standby current; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RP} = t_{RP(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	1390	1210	1120	mA	
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W*	1678	1588	1408	mA	
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1678	1588	1408	mA	
Burst refresh current; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	4270	4180	4090	mA	
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	126	126	126	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7*	2983	2893	2803	mA	

Notes: IDD specification is based on Micron H-die components.

*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	E6 (DDR2-667)		D5 (DDR2-533)		CC (DDR2-400)		Unit	
		Min	Max	Max	Min	Max	Min		
Clock Timing									
Clock Cycle Time	CL5	$t_{CK(5)}$	3000	8000	3750	8000	-	-	ps
	CL4	$t_{CK(4)}$	3750	8000	3750	8000	5000	8000	ps
	CL3	$t_{CK(3)}$	5000	8000	5000	8000	5000	8000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
CK low-level width		$t_{CL(avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
Half clock period		t_{HP}	MIN (t_{CH} , t_{CL})	-	MIN (t_{CH} , t_{CL})	-	MIN (t_{CH} , t_{CL})	-	ps
Clock jitter		t_{JIT}	-125	125	-125	125	-125	125	ps
Data Timing									
DQ output access time from CK/CK#		t_{AC}	-450	+450	-500	500	-600	600	ps
Data-out high impedance window from CK/CK#		t_{HZ}	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		t_{LZ}	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		t_{DS}	100	-	100	-	150	-	ps
DQ and DM input hold time relative to DQS		t_{DH}	175	-	225	-	275	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35	-	0.35	-	0.35	-	t_{CK}
Data hold skew factor		t_{QHS}	-	340	-	400	-	450	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	ps
Data valid output window (DVW)		t_{DVW}	$t_{QH} - t_{DQSQ}$	-	$t_{QH} - t_{DQSQ}$	-	$t_{QH} - t_{DQSQ}$	-	ns
Data Strobe Timing									
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS output access time from CK/CK#		t_{DQSC}	-400	+400	-450	+450	-500	+500	ps
DQS failing edge to CK rising-setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS failing edge from CK rising-hold time		t_{DSH}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	240	-	300	-	350	ps
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read preamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS read preamble setup time		t_{WPRES}	0	-	0	-	0	-	ps
DQS read preamble		t_{WPRE}	0.35	-	0.25	-	0.25	-	t_{CK}
DQS read preamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Write command to first DQS latching transition		t_{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}

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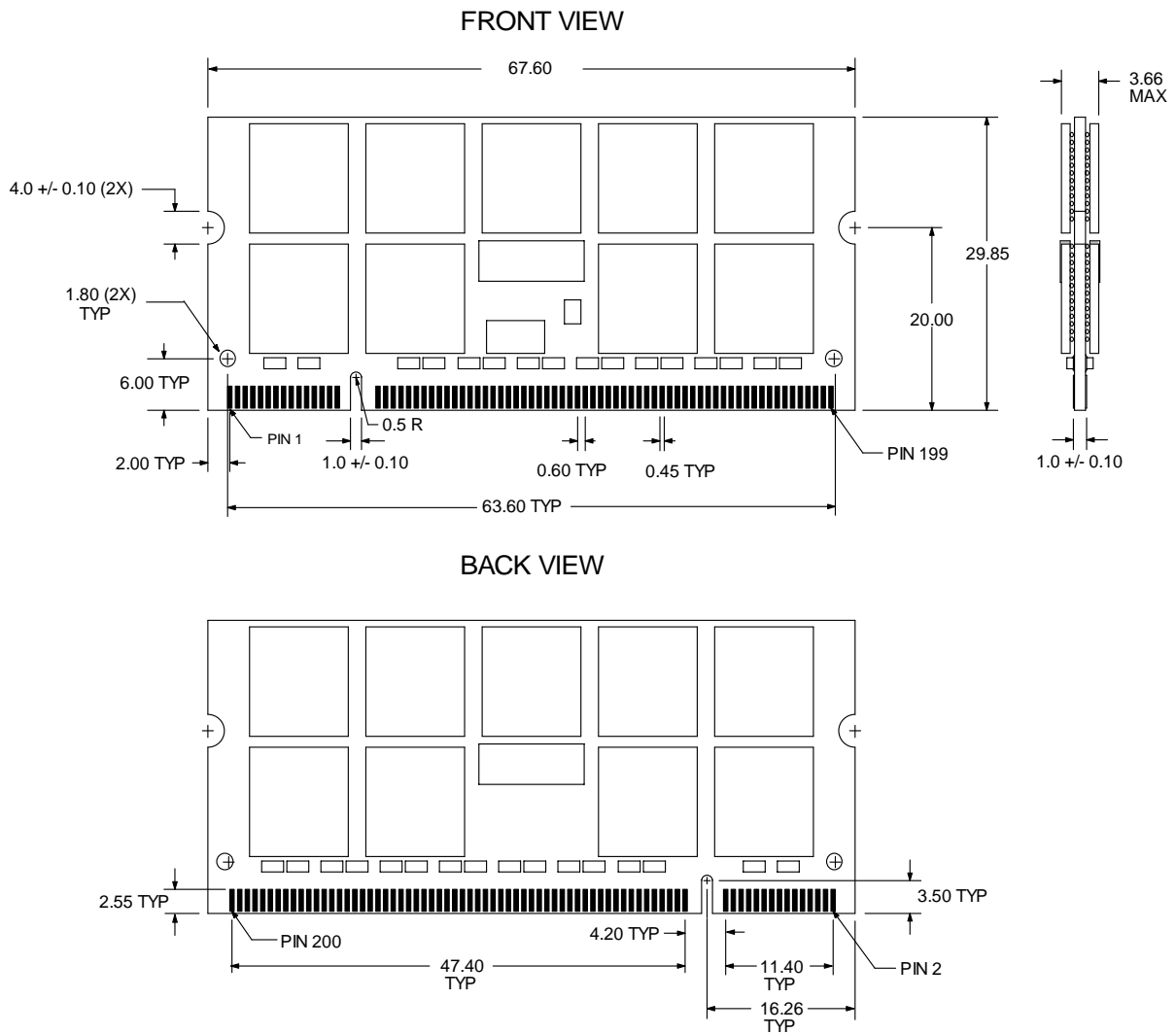
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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	E6 (DDR2-667)		D5 (DDR2-533)		CC (DDR2-400)		Unit
		Min	Max	Min	Max	Min	Max	
Command and Address Timing								
Address and control input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	t_{CK}
Address and control input setup time	t_{IS}	200	-	250	-	350	-	ps
Address and control input hold time	t_{IH}	275	-	375	-	475	-	ps
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	2	-	t_{CK}
ACTIVE to ACTIVE (same bank) command	t_{RC}	55	-	55	-	55	-	ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	15	-	ns
Four Bank Activate period	t_{FAW}	37.5	-	37.5	-	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	ns
Internal READ to precharge Command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns
Write recovery time	t_{WR}	15	-	15	-	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	t_{CK}
Internal WRITE to READ Command delay	t_{WTR}	7.5	-	7.5	-	10	-	ns
PRECHARGE command period	t_{RP}	15	-	15	-	15	-	ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP}+t_{CK}$	-	$t_{RP}+t_{CK}$	-	$t_{RP}+t_{CK}$	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	ns
Self Refresh								
Refresh to Active or Refresh to Refresh command interval	t_{RFC}	127.5	-	127.5	-	127.5	-	ns
Average periodic Refresh interval	t_{REFI}	-	7.8	-	7.8	-	7.8	us
Exit Self Refresh to non-READ command	t_{XSNR}	$t_{RFC(MIN)}+10$	-	$t_{RFC(MIN)}+10$	-	$t_{RFC(MIN)}+10$	-	ns
Exit Self Refresh to READ	t_{XSRD}	200	-	200	-	200	-	t_{CK}
Exit Self Refresh timing reference	t_{ISXR}	t_{IS}	-	t_{IS}	-	t_{IS}	-	ps
ODT								
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)}+700$	$t_{AC(MIN)}$	$t_{AC(MAX)}+1000$	$t_{AC(MIN)}$	$t_{AC(MAX)}+1000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	ps
ODT turn-on(power-down mode)	t_{AONPD}	$t_{AC(MIN)}+2000$	$2 \times t_{CK} + t_{AC(MAX)}+1000$	$t_{AC(MIN)}+2000$	$2 \times t_{CK} + t_{AC(MAX)}+1000$	$t_{AC(MIN)}+2000$	$2 \times t_{CK} + t_{AC(MAX)}+1000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{AC(MIN)}+2000$	$2.5 \times t_{CK} + t_{AC(MAX)}+1000$	$t_{AC(MIN)}+2000$	$2.5 \times t_{CK} + t_{AC(MAX)}+1000$	$t_{AC(MIN)}+2000$	$2.5 \times t_{CK} + t_{AC(MAX)}+1000$	ps
ODT to power-down entry latency	t_{ANPD}	3	-	3	-	3	-	t_{CK}
ODT power-down exit latency	t_{AXPD}	8	-	8	-	8	-	t_{CK}
Power Down								
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	2	-	2	-	t_{CK}
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7-AL	-	6-AL	-	6-AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	2	-	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	3	-	3	-	t_{CK}

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Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only



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Revision History:

Date	Rev.	Page	Changes
04/25/2007	1.0	All	Spec release
06/25/2007	1.1	9	Changed to use millimeter for Package Dimension only
10/01/2007	1.2	1, 9	Changed the height of module as 29.85mm instead of 30mm
12/02/2010	1.3	All	Update datasheet