



Product Specifications

PART NO:

VL491T2863T-E6S/D5S/CCS-I

REV: 1.3

General Information

1GB 128Mx72 DDR2 SDRAM ECC UNBUFFERED SO-CDIMM 200-PIN WITH THERMAL SENSOR

Description: The VL491T2863T is a 128Mx72 DDR2 SDRAM high density SO-CDIMM. This memory module consists of nine CMOS 128Mx8 bit with 8 banks DDR2 Synchronous DRAMs in BGA packages, a zero delay PLL clock in BGA package, and a 2K EEPROM with built-in thermal sensor in 8-pin TSSOP package. This module is a 200-pin dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling

Features

- . 200-pin, small-outline dual in-line memory module (SO-CDIMM)
- . JEDEC pin out
- . Fast data transfer rates: PC2-5300, PC2-4200, & PC2-3200
- . Supports ECC error detection and correction
- . VDD = VDDQ = 1.8V
- . VDDSPD = 3.0V to 3.6V
- . JEDEC standard 1.8V I/O (SSTL_18 compatible)
- . Differential data strobe (DQS, DQS#) option
- . Differential clock inputs (CK, CK#)
- . Four-bit pre-fetch architecture
- . DLL aligns DQ and DQS transition with CK
- . Programmable CAS# latency (CL): 5 (DDR2-667), 4 (DDR2-533), 3 (DDR2-400)
- . Write latency = Read latency - 1tCK
- . Eight internal component banks for concurrent operation
- . Programmable burst; length (4, 8)
- . Adjustable data-output drive strength
- . On-die termination (ODT)
- . Auto & self refresh, (8K/64ms refresh)
- . Serial presence detect (SPD) with EEPROM built-in thermal sensor
- . Thermal sensor range: -20°C to +125°C (+/- 1°C accuracy)
- . Gold edge contacts
- . Lead-free RoHS
- . PCB: Height 30.00mm (1.181"), double sided components
- . Operating temperature (T_{OPER}): -40°C to +85°C (module screening using commercial DRAM)

| Pin Name | Function |
|-------------|---------------------------------|
| A0~A13 | Address Inputs |
| BA0~BA2 | Bank Address Inputs |
| DQ0~DQ63 | Data Input/Output |
| CB0~CB7 | Check Bits |
| DQS0~DQS8 | Data Strobes |
| DQS0#~DQS8# | Data Strobes Complement |
| ODT0 | On-die Termination Control |
| CK,CK# | Clock Input |
| CKE0 | Clock Enables |
| CS0# | Chip Selects |
| RAS# | Row Address Strobes |
| CAS# | Column Address Strobes |
| WE# | Write Enable |
| RESET# | Register Reset Input |
| DM0~DM8 | Data Masks |
| VDD | Voltage Supply 1.8V +/- 0.1V |
| A10/AP | Address Input/Autoprecharge |
| VDDSPD | SPD Voltage supply 3.0V to 3.6V |
| VSS | Ground |
| EVENT# | Temperature Sensor Alarm Output |
| SA0~SA1 | SPD Address |
| SDA | SPD Data Input/Output |
| SCL | SPD Clock Input |
| VREF | SSTL_18 Reference Voltage |
| NC | No Connect |

Order Information:

VL491T2863T-E6 X X - I

- I: Screening temperature
- DRAM DIE (Option)
- DRAM MANUFACTURER
S - SAMSUNG
- MODULE SPEED
E6: PC2-5300 @ CL5
D5: PC2-4200 @ CL4
CC: PC2-3200 @ CL3
- VL : Lead-free/RoHS



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Pin Configuration

| 200-PIN DDR2 SO-CDIMM FRONT | | | | | | | | 200-PIN DDR2 SO-CDIMM BACK | | | | | | | |
|-----------------------------|-------|-----|-------------|-----|-------------|-----|--------|----------------------------|--------|-----|------|-----|------|-----|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | | |
| 1 | VREF | 51 | DQ18 | 101 | VDD | 151 | VSS | 2 | VSS | 52 | VSS | 102 | A6 | 152 | VSS |
| 3 | DQ0 | 53 | DQ19 | 103 | A5 | 153 | DQS5# | 4 | DQ4 | 54 | DQ28 | 104 | A4 | 154 | DM5 |
| 5 | VSS | 55 | VSS | 105 | A3 | 155 | DQS5 | 6 | DQ5 | 56 | DQ29 | 106 | VDD | 156 | VSS |
| 7 | DQ1 | 57 | DQ24 | 107 | A2 | 157 | VSS | 8 | VSS | 58 | VSS | 108 | A1 | 158 | DQ46 |
| 9 | DQS0# | 59 | DQ25 | 109 | VDD | 159 | DQ42 | 10 | DM0 | 60 | DM3 | 110 | A0 | 160 | DQ47 |
| 11 | DQS0 | 61 | VSS | 111 | A10/AP | 161 | DQ43 | 12 | VSS | 62 | VSS | 112 | BA1 | 162 | VSS |
| 13 | VSS | 63 | DSQ3# | 113 | BA0 | 163 | VSS | 14 | DQ6 | 64 | DQ30 | 114 | VDD | 164 | DQ52 |
| 15 | DQ2 | 65 | DSQ3 | 115 | RAS# | 165 | DQ48 | 16 | DQ7 | 66 | DQ31 | 116 | WE# | 166 | DQ53 |
| 17 | DQ3 | 67 | VSS | 117 | VDD | 167 | DQ49 | 18 | VSS | 68 | VSS | 118 | CS0# | 168 | VSS |
| 19 | VSS | 69 | DQ26 | 119 | CAS# | 169 | VSS | 20 | DQ12 | 70 | CB4 | 120 | ODT0 | 170 | DM6 |
| 21 | DQ8 | 71 | DQ27 | 121 | NC/ CS1# | 171 | DQS6# | 22 | DQ13 | 72 | CB5 | 122 | A13 | 172 | VSS |
| 23 | DQ9 | 73 | VSS | 123 | VDD | 173 | DQS6 | 24 | VSS | 74 | VSS | 124 | VDD | 174 | DQ54 |
| 25 | VSS | 75 | CB0 | 125 | NC/ ODT1 | 175 | VSS | 26 | DM1 | 76 | DM8 | 126 | CK | 176 | DQ55 |
| 27 | DQS1# | 77 | CB1 | 127 | NC/ CS3# | 177 | DQ50 | 28 | VSS | 78 | VSS | 128 | CK# | 178 | VSS |
| 29 | DSQ1 | 79 | VSS | 129 | DQ32 | 179 | DQ51 | 30 | DQ14 | 80 | CB6 | 130 | VSS | 180 | DQ60 |
| 31 | VSS | 81 | DQS8# | 131 | VSS | 181 | VSS | 32 | DQ15 | 82 | CB7 | 132 | DQ36 | 182 | DQ61 |
| 33 | DQ10 | 83 | DQS8 | 133 | DQ33 | 183 | DQ56 | 34 | VSS | 84 | VSS | 134 | DQ37 | 184 | VSS |
| 35 | DQ11 | 85 | VSS | 135 | DQS4# | 185 | DQ57 | 36 | DQ20 | 86 | CB2 | 136 | VSS | 186 | DM7 |
| 37 | VSS | 87 | CKE0 | 137 | DQS4 | 187 | VSS | 38 | DQ21 | 88 | CB3 | 138 | DM4 | 188 | DQ62 |
| 39 | DQ16 | 89 | NC/ CKE1 | 139 | VSS | 189 | DQS7# | 40 | VSS | 90 | VSS | 140 | VSS | 190 | VSS |
| 41 | DQ17 | 91 | EVENT# | 141 | DQ34 | 191 | DQS7 | 42 | RESET# | 92 | BA2 | 142 | DQ38 | 192 | DQ63 |
| 43 | VSS | 93 | VDD | 143 | DQ35 | 193 | DQ58 | 44 | DM2 | 94 | NC | 144 | DQ39 | 194 | SDA |
| 45 | DQS2# | 95 | A12 | 145 | VSS | 195 | VSS | 46 | VSS | 96 | A11 | 146 | VSS | 196 | SCL |
| 47 | DQS2 | 97 | A9 | 147 | DQ40 | 197 | DQ59 | 48 | DQ22 | 98 | VDD | 148 | DQ44 | 198 | SA1 |
| 49 | VSS | 99 | A7 | 149 | DQ41 | 199 | VDDSPD | 50 | DQ23 | 100 | A8 | 150 | DQ45 | 200 | SA0 |

Note: 1. NC/CS2#, NC/CS3# (pins 91, 127) are used for 4 rank module
 2. NC/CS1# (pin 121), NC/CKE1 (pin 89), NC/ODT1 (pin 125) are used for 2 rank module



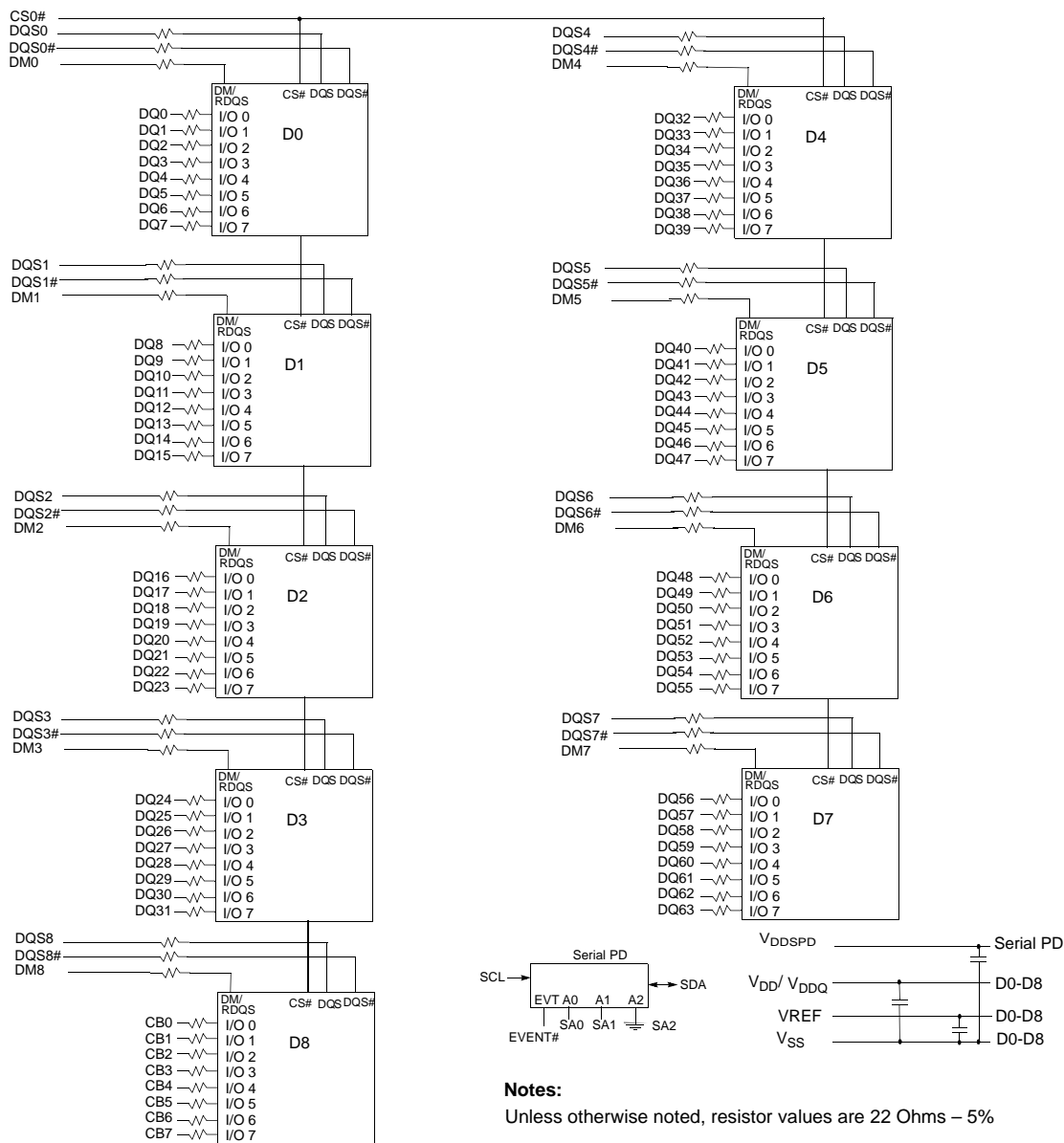
Product Specifications

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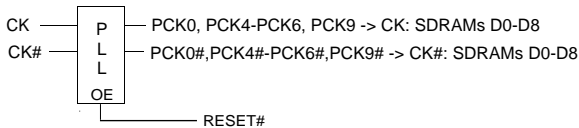
VL491T2863T-E6S/D5S/CCS-I

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Functional Block Diagram



- CS0# → CS0#: SDRAMs D0-D8
- BA0-BA2 → BA0-BA2: SDRAMs D0-D8
- A0-A13 → A0-A13: SDRAMs D0-D8
- RAS# → RAS#: SDRAMs D0-D8
- CAS# → CAS#: SDRAMs D0-D8
- WE# → WE# : SDRAMs D0-D8
- CKE0 → CKE0 : SDRAMs D0-D8
- ODT0 → ODT0: SDRAMs D0-D8





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Absolute Maximum Ratings

| Symbol | Parameter | MIN | MAX | Unit | |
|-----------|--|--------------------------------------|------|------|----|
| VDD | Voltage on VDD pin relative to Vss | -1.0 | 2.3 | V | |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.5 | 2.3 | V | |
| VDDL | Voltage on VDDL pin relative to Vss | -0.5 | 2.3 | V | |
| VIN, VOUT | Voltage on any pin relative to Vss | -0.5 | 2.3 | V | |
| TSTG | Storage temperature | -55 | 100 | °C | |
| IL | Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V | Command/Address, RAS#, CAS#, WE#, BA | -45 | 45 | uA |
| | | CS#, CKE, ODT | -45 | 45 | uA |
| | | CK, CK# | -250 | 250 | uA |
| | | DM | -5 | 5 | uA |
| Ioz | Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled | DQ, DQS, DQS# | -5 | 5 | uA |
| IREF | VREF leakage current; VREF = Valid VREF level | -18 | 18 | uA | |

DC Operating Conditions

All voltages referenced to VSS

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|-------------------------|--------|-------------|-------------|-------------|------|-------|
| Supply voltage | VDD | 1.7 | 1.8 | 1.9 | V | 1 |
| I/O Supply voltage | VDDQ | 1.7 | 1.8 | 1.9 | V | 4 |
| VDDL Supply voltage | VDDL | 1.7 | 1.8 | 1.9 | V | 4 |
| I/O Reference voltage | VREF | 0.49 x VDDQ | 0.50 x VDDQ | 0.51 x VDDQ | V | 2 |
| I/O Termination voltage | VTT | VREF-0.04 | VREF | VREF+0.04 | V | 3 |

- Notes:
1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
 2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
 3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
 4. VDDQ tracks with VDD; VDDL tracks with VDD.



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Operating Temperature Condition

| Parameter | Symbol | Rating | Units | Notes |
|-----------------------|--------|------------|-------|-------|
| Operating temperature | TOPER | -40 to +85 | °C | 1, 2 |

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
- At -40°C to + 85°C, operation temperature range, all DRAM specifications will be supported.

Input DC Logic Level

All voltages referenced to VSS

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|---------|--------------|--------------|------|
| Input High (Logic 1) Voltage | VIH(DC) | VREF + 0.125 | VDDQ + 0.300 | V |
| Input Low (Logic 0) Voltage | VIL(DC) | -0.300 | VREF - 0.125 | V |

Input AC Logic Level

All voltages referenced to VSS

| Parameter | Symbol | Min | Max | Unit |
|---|---------|--------------|--------------|------|
| AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533 | VIH(AC) | VREF + 0.250 | - | V |
| AC Input High (Logic 1) Voltage DDR2-667 | VIH(AC) | VREF + 0.200 | - | V |
| AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533 | VIL(AC) | - | VREF - 0.250 | V |
| AC Input Low (Logic 0) Voltage DDR2-667 | VIL(AC) | - | VREF - 0.200 | V |

Input/Output Capacitance

TA=25°C, f=100MHz

| Parameter | Symbol | Min | Max | Unit |
|--|----------------|-----|-----|------|
| Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#) | CIN1 | 13 | 22 | pF |
| Input capacitance (CKE0), (ODT0) | CIN2 | 13 | 22 | pF |
| Input capacitance (CS0#) | CIN3 | 13 | 22 | pF |
| Input capacitance (CK, CK#) | CIN4 | 6 | 7 | pF |
| Input capacitance (DM0 ~ DM8), (CB0 ~ CB7) | CIN5 (E6) | 6.5 | 7.5 | pF |
| | CIN5 (D5, CC) | 6.5 | 8 | pF |
| Input capacitance (DQ0 ~ DQ63), (DQS0 ~ DQS8) | COUT1 (E6) | 6.5 | 7.5 | pF |
| | COUT1 (D5, CC) | 6.5 | 8 | pF |



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IDD Specification

| Condition | Symbol | E6 (DDR2-667) | D5 (DDR2-533) | CC (DDR2-400) | Unit |
|---|---------------------------|---------------------------|------------------|------------------|------|
| Operating one bank active-precharge; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD0 | 1110 | 1065 | 1020 | mA |
| Operating one bank active-read-precharge; IOUT = 0mA; BL = 4; CL = CL(IDD); $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is same as IDD4W. | IDD1 | 1200 | 1155 | 1110 | mA |
| Precharge power-down current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2P | 408 | 408 | 408 | mA |
| Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2Q | 660 | 615 | 615 | mA |
| Precharge standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING. | IDD2N | 705 | 660 | 660 | mA |
| Active power-down current; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. | Fast PDN Exit MRS(12) = 0 | 570 | 525 | 525 | mA |
| | | Slow PDN Exit MRS(12) = 1 | 408 | 408 | 408 |
| Active standby current; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD3N | 750 | 705 | 705 | mA |
| Operating burst write current; All banks open; Continuous burst writes; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD4W | 1695 | 1470 | 1335 | mA |
| Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W. | IDD4R | 1695 | 1470 | 1335 | mA |
| Burst auto refresh current; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD5 | 2280 | 2235 | 2190 | mA |
| Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. | Normal | 90 | 90 | 90 | mA |
| Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING. | IDD7 | 3000 | 2820 | 2640 | mA |

Note: IDD specification is based on Samsung components. Other DRAM Manufacturers specification may be different.



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AC Timing Parameters & Specifications

| Parameter | Symbol | E6 (DDR2-667) | | D5 (DDR2-533) | | CC (DDR2-400) | | Unit | | |
|--|--|-----------------------------|---------------------|-----------------------------|---------------------|-----------------------------|---------------------|---------------|----------|----------|
| | | Min | Max | Min | Max | Min | Max | | | |
| Clock | Clock cycle time | CL=5 | $t_{CK}(5)$ | 3000 | 8000 | - | - | - | - | ps |
| | | CL=4 | $t_{CK}(4)$ | 3750 | 8000 | 3,750 | 8,000 | 5,000 | 8,000 | ps |
| | | CL=3 | $t_{CK}(3)$ | 5000 | 8000 | 5,000 | 8,000 | 5,000 | 8,000 | ps |
| | CK high-level width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | |
| | CK low-level width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | |
| Half clock period | t_{HP} | MIN (t_{CH}, t_{CL}) | | MIN (t_{CH}, t_{CL}) | | MIN (t_{CH}, t_{CL}) | | | ps | |
| Clock jitter | t_{JIT} | -125 | 125 | -125 | 125 | -125 | 125 | | ps | |
| Data | DQ output access time from CK/CK# | t_{AC} | -450 | +450 | -500 | +500 | -600 | +600 | | ps |
| | Data-out high impedance window from CK/CK# | t_{HZ} | | $t_{AC}(MAX)$ | | $t_{AC}(MAX)$ | | $t_{AC}(MAX)$ | | ps |
| | Data-out low-impedance window from CK/CK# | t_{LZ} | $t_{AC}(MIN)$ | $t_{AC}(MAX)$ | $t_{AC}(MIN)$ | $t_{AC}(MAX)$ | $t_{AC}(MIN)$ | $t_{AC}(MAX)$ | | ps |
| | DQ and DM input setup time relative to DQS | t_{DS} | 100 | | 100 | | 150 | | | |
| | DQ and DM input hold time relative to DQS | t_{DH} | 175 | | 225 | | 275 | | | |
| | DQ and DM input pulse width (for each input) | t_{DIPW} | 0.35 | | 0.35 | | 0.35 | | | t_{CK} |
| | Data hold skew factor | t_{QHS} | | 340 | | 400 | | 450 | | ps |
| | DQ-DQS hold, DQS to first DQ to go nonvalid, per access | t_{QH} | $t_{HP} - t_{QHS}$ | | $t_{HP} - t_{QHS}$ | | $t_{HP} - t_{QHS}$ | | | ps |
| | Data valid output window (DVW) | t_{DVW} | $t_{QH} - t_{DQSQ}$ | | $t_{QH} - t_{DQSQ}$ | | $t_{QH} - t_{DQSQ}$ | | | ns |
| Data Strobe | DQS input high pulse width | t_{DQSH} | 0.35 | | 0.35 | | 0.35 | | | t_{CK} |
| | DQS input low pulse width | t_{DQSL} | 0.35 | | 0.35 | | 0.35 | | | t_{CK} |
| | DQS output access time from CK/CK# | t_{DQSCK} | -400 | +400 | -450 | +450 | -500 | +500 | | ps |
| | DQS falling edge to CK rising – setup time | t_{DSS} | 0.2 | | 0.2 | | 0.2 | | | t_{CK} |
| | DQS falling edge from CK rising – hold time | t_{DSH} | 0.2 | | 0.2 | | 0.2 | | | t_{CK} |
| | DQS-DQ skew, DQS to last DQ valid, per group, per access | t_{DQSQ} | | 240 | | 300 | | 350 | | ps |
| | DQS read preamble | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | | t_{CK} |
| | DQS read postamble | t_{RPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | | t_{CK} |
| | DQS write preamble setup time | t_{WPRES} | 0 | | 0 | | 0 | | | ps |
| | DQS write preamble | t_{WPRE} | 0.35 | | 0.35 | | 0.35 | | | t_{CK} |
| | DQS write postamble | t_{WPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | | t_{CK} |
| Write command to first DQS latching transition | t_{DQSS} | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | WL-0.25 | WL+0.25 | | t_{CK} | |



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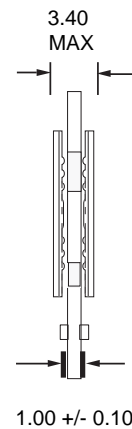
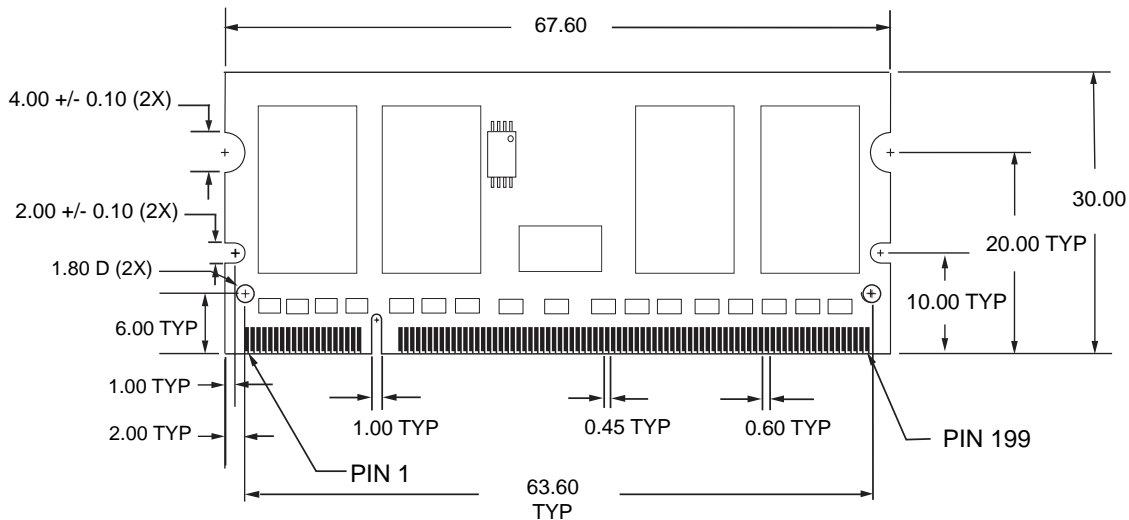
AC Timing Parameters & Specifications (cont')

| Parameter | Symbol | E6 (DDR2-667) | | D5 (DDR2-533) | | CC (DDR2-400) | | Unit | |
|---------------------|--|------------------|------------------------|---|------------------------|---|------------------------|---|----------|
| | | Min | Max | Min | Max | Min | Max | | |
| Command and Address | Address and control input pulse width for each input | t_{PW} | 0.6 | | 0.6 | | 0.6 | | t_{CK} |
| | Address and control input setup time | t_{IS} | 200 | | 250 | | 350 | | ps |
| | Address and control input hold time | t_{IH} | 275 | | 375 | | 475 | | ps |
| | CAS# to CAS# command delay | t_{CCD} | 2 | | 2 | | 2 | | ps |
| | ACTIVE to ACTIVE (same bank) command | t_{RC} | 60 | | 60 | | 55 | | ns |
| | ACTIVE bank a to ACTIVE bank b command | t_{RRD} | 7.5 | | 7.5 | | 7.5 | | ns |
| | ACTIVE to READ or WRITE delay | t_{RCD} | 15 | | 15 | | 15 | | ns |
| | Four Bank Activate period | t_{FAW} | 37.5 | | 37.5 | | 37.5 | | ns |
| | ACTIVE to PRECHARGE command | t_{RAS} | 45 | 70,000 | 45 | 70,000 | 40 | 70,000 | ns |
| | Internal READ to precharge command delay | t_{RTP} | 7.5 | | 7.5 | | 7.5 | | ns |
| | Write recovery time | t_{WR} | 15 | | 15 | | 15 | | ns |
| | Auto precharge write recovery + precharge time | t_{DAL} | $t_{WR}+t_{RP}$ | | $t_{WR}+t_{RP}$ | | $t_{WR}+t_{RP}$ | | ns |
| | Internal WRITE to READ command delay | t_{WTR} | 7.5 | | 7.5 | | 10 | | ns |
| | PRECHARGE command period | t_{RP} | 15 | | 15 | | 15 | | ns |
| | PRECHARGE ALL command period | t_{RPA} | $t_{RP}+t_{CK}$ | | $t_{RP}+t_{CK}$ | | $t_{RP}+t_{CK}$ | | ns |
| | LOAD MODE command cycle time | t_{MRD} | 2 | | 2 | | 2 | | t_{CK} |
| Self Refresh | CKE low to CK,CK# uncertainty | t_{DELAY} | $t_{IS}+t_{CK}+t_{IH}$ | | $t_{IS}+t_{CK}+t_{IH}$ | | $t_{IS}+t_{CK}+t_{IH}$ | | ns |
| | REFRESH to Active or Refresh to Refresh command interval | t_{RFC} | 127.5 | 70,000 | 127.5 | 70,000 | 127.5 | 70,000 | ns |
| | Average periodic refresh interval | t_{REFI} | | 7.8 | | 7.8 | | 7.8 | us |
| | Exit self refresh to non-READ command | t_{XSNR} | $t_{RFC(MIN)}+10$ | | $t_{RFC(MIN)}+10$ | | $t_{RFC(MIN)}+10$ | | ns |
| ODT | Exit self refresh to READ | t_{XSRD} | 200 | | 200 | | 200 | | t_{CK} |
| | Exit self refresh timing reference | t_{ISXR} | t_{IS} | | t_{IS} | | t_{IS} | | ps |
| | ODT turn-on delay | t_{AOND} | 2 | 2 | 2 | 2 | 2 | 2 | t_{CK} |
| | ODT turn-on | t_{AON} | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+700$ | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+1000$ | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+1000$ | ps |
| | ODT turn-off delay | t_{AOFD} | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | t_{CK} |
| | ODT turn-off | t_{AOF} | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+600$ | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+600$ | $t_{AC(MIN)}$ | $t_{AC(MAXI)}+600$ | ps |
| | ODT turn-on (power-down mode) | t_{AONPD} | $t_{AC(MIN)}+2000$ | $2 \times t_{CK} + t_{AC(MAXI)}+1000$ | $t_{AC(MIN)}+2000$ | $2 \times t_{CK} + t_{AC(MAXI)}+1000$ | $t_{AC(MIN)}+2000$ | $2 \times t_{CK} + t_{AC(MAXI)}+1000$ | ps |
| | ODT turn-off (power-down mode) | t_{AOFPD} | $t_{AC(MIN)}+2000$ | $2.5 \times t_{CK} + t_{AC(MAXI)}+1000$ | $t_{AC(MIN)}+2000$ | $2.5 \times t_{CK} + t_{AC(MAXI)}+1000$ | $t_{AC(MIN)}+2000$ | $2.5 \times t_{CK} + t_{AC(MAXI)}+1000$ | ps |
| | ODT to power-down entry latency | t_{ANPD} | 3 | | 3 | | 3 | | t_{CK} |
| | ODT power-down exit latency | t_{AXPD} | 8 | | 8 | | 8 | | t_{CK} |
| Power-Down | Exit active power-down to READ command, MR[bit12=0] | t_{XARD} | 2 | | 2 | | 2 | | t_{CK} |
| | Exit active power-down to READ command, MR[bit12=1] | t_{XARDS} | 7-AL | | 6-AL | | 6-AL | | t_{CK} |
| | Exit precharge power-down to any non-READ command. | t_{XP} | 2 | | 2 | | 2 | | t_{CK} |
| | CKE minimum high/low time | t_{CKE} | 3 | | 3 | | 3 | | t_{CK} |

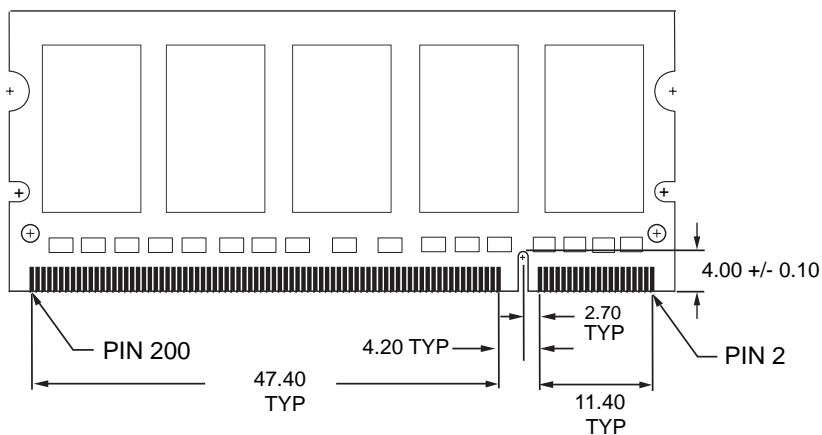
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|---------------------------------|---------------------------|----------|
| <h1>Product Specifications</h1> | | |
| PART NO: | VL491T2863T-E6S/D5S/CCS-I | REV: 1.3 |

Package Dimensions

FRONT VIEW



BACK VIEW



NOTE:

All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.



Product Specifications

PART NO: VL491T2863T-E6S/D5S/CCS-I

REV: 1.3

Revision History:

| Date | Rev. | Page | Changes |
|------------|------|------|---|
| 11/14/2006 | 1.0 | All | Released spec |
| 03/02/2009 | 1.1 | All | Data sheet update |
| 09/02/2010 | 1.2 | 5 | Update Input leak current of PLL clock (IL) |
| 12/20/2010 | 1.3 | 1 | Update General Information |