| Virtium Technology, Inc. | Product Specifications | |
|---|---|---|
| PART NO: | VL47B2863Z-R9S/R8S/R7S-HS | REV: 1.1 |

## General Information

### 1GB 128MX64 DDR3 UNBUFFERED 204 PIN SODIMM HEAT SPREADER AND CONFORMAL COATING

**Description:** The VL47B2863Z is a 128M X 64 DDR3 SDRAM high density SODIMM. This memory module consists of eight CMOS 128Mx8 bit with 8 banks DDR3 Synchronous DRAMs in BGA packages and a 2K EEPROM with Thermal Sensor in an 8-pin MLF package. This module is a 204-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

## Features:

. 204-pin, small-outline dual in-line memory module (SODIMM)
. Fast data transfer rates: PC3-10600, PC3-8500, PC3-6400
. VDD = VDDQ = 1.5V +/- 0.075V
. VDDSPD = 3V to 3.6V
. JEDEC standard 1.5V +/- 0.075V I/O (SSTL_15 compatible)
. 8 Banks
. 8-bit pre-fetch architecture
. Bi-directional Differential Data-Strobe
. Programmable CAS# Latency: 6, 7, 9
. Programmable burst; length (8)
. On-die termination (ODT)
. Average refresh period 7.8 us
. Asynchronous Reset
. Fly-by topology
. Terminated command, address, and control bus
. Gold edge PCB contacts
. Lead-free, RoHS compliant
. Serial presence detect (SPD) with EEPROM with Thermal Sensor
. Thermal sensor range: -20$^0$C to +125$^0$C (+/- 1$^0$C Accuracy)
. JEDEC pin out
. PCB: Height 30mm (1.181”), double sided components
. Conformal coating MIL-I-46058C
. Operating temperature (TOPER): -40$^0$C to +85$^0$C

| Pin Name | Function |
|---|---|
| A0~A13 | Address Inputs |
| A10/AP | Address Input/Auto Precharge |
| BA0~BA2 | Bank Address Inputs |
| DQ0~DQ63 | Data Input/Output |
| DQS0~DQS7 | Data Strobes |
| DQS0#~DQS7# | Data Strobes Complement |
| ODT0 | On-die Termination Control |
| CK0,CK0# | Clock Input |
| CKE0 | Clock Enables |
| CS0# | Chip Selects |
| RAS# | Row Address Strobes |
| CAS# | Column Address Strobes |
| WE# | Write Enable |
| VDD | Voltage Supply 1.5V +/- 0.075V |
| VSS | Ground |
| SA0~SA1 | SPD Address |
| SDA | SPD Data Input/Output |
| SCL | SPD Clock Input |
| DM0~DM7 | Data Masks |
| VREFCA | Reference Voltage for CA |
| VREFDQ | Reference Voltage for DQ |
| VDDSPD | SPD Voltage Supply 3V to 3.6V |
| VTT | Termination Voltage |
| RESET# | Register and SDRAM Control |
| EVENT# | Reserved for Temp Sensing |
| NC | No Connect |

## Order Information:

**VL47B2863Z-R9 S X-HS**

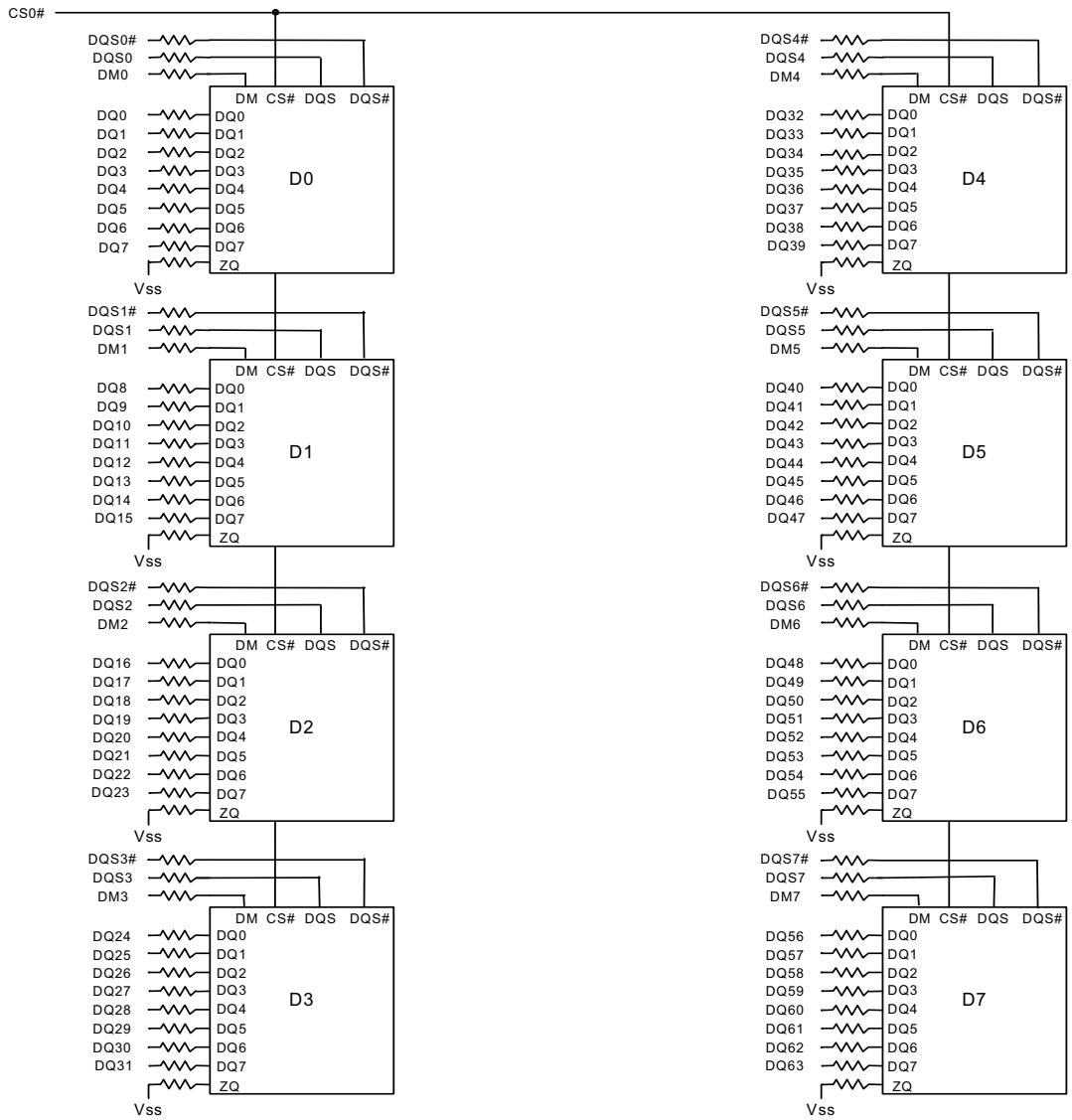
- HS: Heat Sink
- DRAM DIE (option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  R9: PC3-10600 @ CL9
  R8: PC3-8500 @ CL7
  R7: PC3-6400 @ CL6
  (R: Screening grade)
- Conformal coating
- VL: Lead-free/RoHS

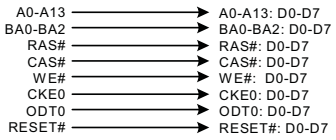
## Pin Configuration

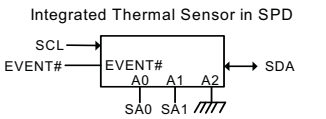
| 204-PIN DDR3 SODIMM FRONT | | | | | | | | 204-PIN DDR3 SODIMM BACK | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | VREFDQ | 53 | DQ19 | 105 | VDD | 157 | DQ42 | 2 | VSS | 54 | VSS | 106 | VDD | 158 | DQ46 |
| 3 | VSS | 55 | VSS | 107 | A10 | 159 | DQ43 | 4 | DQ4 | 56 | DQ28 | 108 | BA1 | 160 | DQ47 |
| 5 | DQ0 | 57 | DQ24 | 109 | BA0 | 161 | VSS | 6 | DQ5 | 58 | DQ29 | 110 | RAS# | 162 | VSS |
| 7 | DQ1 | 59 | DQ25 | 111 | VDD | 163 | DQ48 | 8 | VSS | 60 | VSS | 112 | VDD | 164 | DQ52 |
| 9 | VSS | 61 | VSS | 113 | WE# | 165 | DQ49 | 10 | DQS0# | 62 | DQ3# | 114 | CS0# | 166 | DQ53 |
| 11 | DM0 | 63 | DM3 | 115 | CAS# | 167 | VSS | 12 | DQS0 | 64 | DQ3 | 116 | ODT0 | 168 | VSS |
| 13 | VSS | 65 | VSS | 117 | VDD | 169 | DQS6# | 14 | VSS | 66 | VSS | 118 | VDD | 170 | DM6 |
| 15 | DQ2 | 67 | DQ26 | 119 | A13 | 171 | DQS6 | 16 | DQ6 | 68 | DQ30 | 120 | ODT1* | 172 | VSS |
| 17 | DQ3 | 69 | DQ27 | 121 | CS1#* | 173 | VSS | 18 | DQ7 | 70 | DQ31 | 122 | NC | 174 | DQ54 |
| 19 | VSS | 71 | VSS | 123 | VDD | 175 | DQ50 | 20 | VSS | 72 | VSS | 124 | VDD | 176 | DQ55 |
| 21 | DQ8 | 73 | CKE0 | 125 | NC | 177 | DQ51 | 22 | DQ12 | 74 | CKE1* | 126 | VREFCA | 178 | VSS |
| 23 | DQ9 | 75 | VDD | 127 | VSS | 179 | VSS | 24 | DQ13 | 76 | VDD | 128 | VSS | 180 | DQ60 |
| 25 | VSS | 77 | NC | 129 | DQ32 | 181 | DQ56 | 26 | VSS | 78 | NC | 130 | DQ36 | 182 | DQ61 |
| 27 | DQS1# | 79 | BA2 | 131 | DQ33 | 183 | DQ57 | 28 | DM1 | 80 | NC/A14 | 132 | DQ37 | 184 | VSS |
| 29 | DQS1 | 81 | VDD | 133 | VSS | 185 | VSS | 30 | RESET# | 82 | VDD | 134 | VSS | 186 | DQS7# |
| 31 | VSS | 83 | A12 | 135 | DQS4# | 187 | DM7 | 32 | VSS | 84 | A11 | 136 | DM4 | 188 | DQS7 |
| 33 | DQ10 | 85 | A9 | 137 | DQS4 | 189 | VSS | 34 | DQ14 | 86 | A7 | 138 | VSS | 190 | VSS |
| 35 | DQ11 | 87 | VDD | 139 | VSS | 191 | DQ58 | 36 | DQ15 | 88 | VDD | 140 | DQ38 | 192 | DQ62 |
| 37 | VSS | 89 | A8 | 141 | DQ34 | 193 | DQ59 | 38 | VSS | 90 | A6 | 142 | DQ39 | 194 | DQ63 |
| 39 | DQ16 | 91 | A5 | 143 | DQ35 | 195 | VSS | 40 | DQ20 | 92 | A4 | 144 | VSS | 196 | VSS |
| 41 | DQ17 | 93 | VDD | 145 | VSS | 197 | SA0 | 42 | DQ21 | 94 | VDD | 146 | DQ44 | 198 | EVENT# |
| 43 | VSS | 95 | A3 | 147 | DQ40 | 199 | VDDSPD | 44 | VSS | 96 | A2 | 148 | DQ45 | 200 | SDA |
| 45 | DQS2# | 97 | A1 | 149 | DQ41 | 201 | SA1 | 46 | DM2 | 98 | A0 | 150 | VSS | 202 | SCL |
| 47 | DQS2 | 99 | VDD | 151 | VSS | 203 | VTT | 48 | VSS | 100 | VDD | 152 | DQS5# | 204 | VTT |
| 49 | VSS | 101 | CK0 | 153 | DM5 | | | 50 | DQ22 | 102 | CK1* | 154 | DQS5 | | |
| 51 | DQ18 | 103 | CK0# | 155 | VSS | | | 52 | DQ23 | 104 | CK1#* | 156 | VSS | | |

Notes: 1. Pin 80 is NC for 1GB and A14 for 2GB component.
2. * These pins are not used in this module.

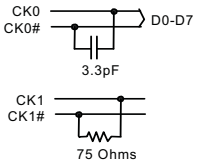
## Functional Block Diagram



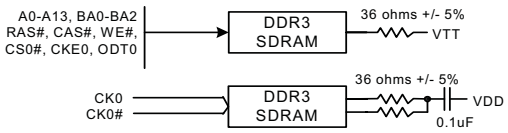



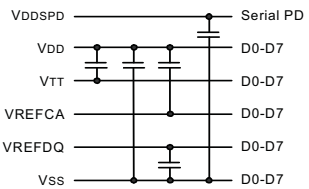




Serial PD with Integrated thermal sensor




Command, address, control, and clock line terminations




Notes:
1. Unless otherwise noted, resistor values are 15 Ohms +/- 5%
2. ZQ resistors are 240 Ohms +/- 1%

## Absolute Maximum Ratings

| Symbol | Parameter | | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | | -0.4 | 1.975 | V |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | | -0.4 | 1.975 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | | -0.4 | 1.975 | V |
| $T_{STG}$ | Storage temperature | | -55 | 100 | $^0$C |
| $I_L$ | Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V | Command/Address, RAS#, CAS#, WE#, CS#, CKE, ODT, BA | -16 | 16 | uA |
| | | CK, CK# | -16 | 16 | uA |
| | | DM | -2 | 2 | uA |
| $I_{OZ}$ | Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled | DQ, DQS, DQS# | -5 | 5 | uA |
| $I_{VREF}$ | VREF leakage current; VREF = Valid VREF level | | -8 | 8 | uA |

## DC Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | 1.425 | 1.5 | 1.575 | V | 1,2 |
| Supply Voltage for Output | VDDQ | 1.425 | 1.5 | 1.575 | V | 1,2 |
| I/O Reference voltage (DQ) | VREFDQ (DC) | 0.49 x VDDQ | 0.5 x VDD | 0.51 x VDDQ | V | 3,4 |
| I/O Reference voltage (CMD/ADD) | VREFCA (DC) | 0.49 x VDDQ | 0.5 x VDD | 0.51 x VDDQ | V | 3,4 |
| Termination Reference Voltage | VTT | -0.483 x VDD | 0.5 x VDD | +0.517 x VDD | V | 5 |

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD andVDDQ tied together.
3. The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/- 1% VDD.
4. For reference: approximate VDD/2 +/- 15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

## Operating Temperature Condition

| Parameter | Symbol | Rating | Units | Notes |
|---|---|---|---|---|
| Operating temperature | $T_{OPER}$ | -40 to +85 | $^0$C | 1,2 |

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD5-2
2. At -40 to +85$^0$C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85$^0$C < $T_{OPER}$ <= 95$^0$C

## Input DC Logic Level

All voltages referenced to VSS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **Command and Address** | | | | |
| Input High (Logic 1) Voltage DDR3-800/1066/1333 | VIHCA(DC) | VREF + 0.100 | VDD | V |
| Input Low (Logic 0) Voltage DDR3-800/1066/1333 | VILCA(DC) | VSS | VREF - 0.100 | V |
| **DQ and DM** | | | | |
| Input High (Logic 1) Voltage DDR3-800/1066/1333 | VIHDQ(DC) | VREF + 0.100 | VDD | V |
| Input Low (Logic 0) Voltage DDR3-800/1066/1333 | VILDQ(DC) | VSS | VREF - 0.100 | V |

## Input AC Logic Level

All voltages referenced to VSS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **Command and Address** | | | | |
| AC Input High (Logic 1) Voltage DDR3-800/1066/1333 | VIHCA(AC) | VREF + 0.175 | - | V |
| AC Input Low (Logic 0) Voltage DDR3-800/1066/1333 | VILCA(AC) | - | VREF - 0.175 | V |
| **DQ and DM** | | | | |
| AC Input High (Logic 1) Voltage DDR3-800/1066 | VIHDQ(AC) | VREF + 0.175 | - | V |
| AC Input Low (Logic 0) Voltage DDR3-800/1066 | VILDQ(AC) | - | VREF - 0.175 | V |
| AC Input High (Logic 1) Voltage DDR3-1333 | VIHDQ(AC) | VREF + 0.150 | - | V |
| AC Input Low (Logic 0) Voltage DDR3-1333 | VILDQ(AC) | - | VREF - 0.150 | V |

## Input/Output Capacitance

TA=25$^0$C, f=100MHz

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance (A0~A13, BA0~BA2,RAS#,CAS#,WE#) | CIN1 | 10 | 16 | pF |
| Input capacitance (CKE0), (ODT0), (CS0#) | CIN2 | 10 | 16 | pF |
| Input capacitance (CK0, CK0#) | CIN3 | 10.4 | 16.8 | pF |
| Input/Output capacitance (DM0~DM7), (DQ0~DQ63), (DQS0~DQS7) | CIO | 5.5 | 7 | pF |
| Input/Output capacitance of ZQ pin | CZQ | - | 28 | pF |

## IDD Specification

| Condition | Symbol | DDR3-1333 | DDR3-1066 | DDR3-800 | Unit |
|---|---|---|---|---|---|
| **Operating one bank active-precharge current;** $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD0 | 760 | 720 | 640 | mA |
| **Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W. | IDD1 | 920 | 880 | 800 | mA |
| **Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2P-F | 80 | 80 | 80 | mA |
| | IDD2P-S | 80 | 80 | 80 | mA |
| **Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD2N | 360 | 320 | 280 | mA |
| **Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2Q | 360 | 320 | 280 | mA |
| **Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. | IDD3P | 480 | 400 | 360 | mA |
| **Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RP} = t_{RP(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD3N | 640 | 520 | 480 | mA |
| **Operating burst read current**; All banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W. | IDD4R | 1680 | 1360 | 1120 | mA |
| **Operating burst write current**; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD4W | 1600 | 1280 | 1040 | mA |
| **Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD5 | 1840 | 1680 | 1680 | mA |
| **Self refresh current;** CK and CK# at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. | IDD6 | 80 | 80 | 80 | mA |
| **Operating bank interleave read current;** All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R. | IDD7 | 2560 | 2160 | 2000 | mA |

Note: IDD specification is based on Samsung D-die components.

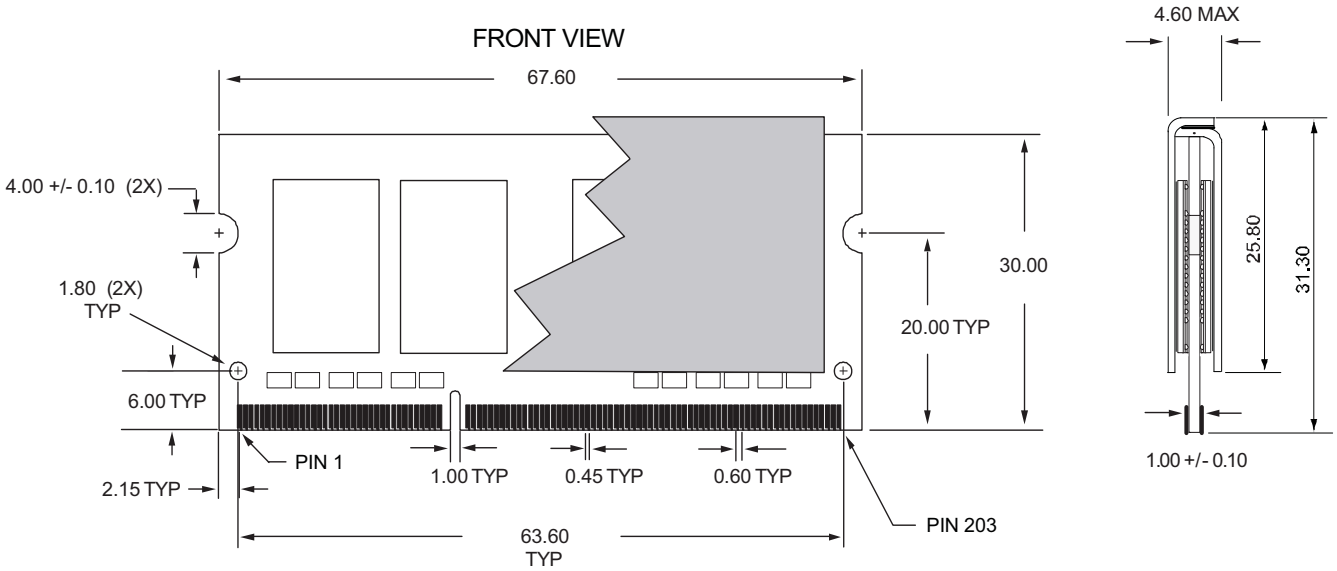
| AC TIMING PARAMETERS & SPECIFICATIONS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | DDR3-1333 | | DDR3-1066 | | DDR3-800 | | Unit |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **Clock Timing** | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK(DLL_OFF) | 8 | - | 8 | - | 8 | - | ns |
| Average Clock Period | tCK(avg) | See Speed Bins Table | | | | | | ps |
| Clock Period | tCK(abs) | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | ps |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) |
| Clock Period Jitter (Period) | tJIT(per) | -80 | 80 | -90 | 90 | -100 | 100 | ps |
| Clock Period Jitter during DLL locking period | tJIT(per, lck) | -70 | 70 | -80 | 80 | -90 | 90 | ps |
| Cycle to Cycle Period Jitter | tJIT(cc) | 160 | | 180 | | 200 | | ps |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc, lck) | 140 | | 160 | | 180 | | ps |
| Cumulative error across 2 cycles | tERR(2per) | -118 | 118 | -132 | 132 | -147 | 147 | ps |
| Cumulative error across 3 cycles | tERR(3per) | -140 | 140 | -157 | 157 | -175 | 175 | ps |
| Cumulative error across 4 cycles | tERR(4per) | -155 | 155 | -175 | 175 | -194 | 194 | ps |
| Cumulative error across 5 cycles | tERR(5per) | -168 | 168 | -188 | 188 | -209 | 209 | ps |
| Cumulative error across 6 cycles | tERR(6per) | -177 | 177 | -200 | 200 | -222 | 222 | ps |
| Cumulative error across 7 cycles | tERR(7per) | -186 | 186 | -209 | 209 | -232 | 232 | ps |
| Cumulative error across 8 cycles | tERR(8per) | -193 | 193 | -217 | 217 | -241 | 241 | ps |
| Cumulative error across 9 cycles | tERR(9per) | -200 | 200 | -224 | 224 | -249 | 249 | ps |
| Cumulative error across 10 cycles | tERR(10per) | -205 | 205 | -231 | 231 | -257 | 257 | ps |
| Cumulative error across 11 cycles | tERR(11per) | -210 | 210 | -237 | 237 | -263 | 263 | ps |
| Cumulative error across 12 cycles | tERR(12per) | -215 | 215 | -242 | 242 | -269 | 269 | ps |
| Cumulative error across n = 13, 14 ... 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min<br>tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max | | | | | | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | | 0.43 | | 0.43 | | tCK(avg) |
| Absolute clock Low pulse width | tCL(abs) | 0.43 | | 0.43 | | 0.43 | | tCK(avg) |
| **Data Timing** | | | | | | | | |
| DQS,DQS to DQ skew, per group, per access | tDQSQ | - | 125 | - | 150 | - | 200 | ps |
| DQ output hold time from DQS, DQS | tQH | 0.38 | - | 0.38 | - | 0.38 | - | tCK(avg) |
| DQ low-impedance time from CK, CK | tLZ(DQ) | -500 | 250 | -600 | 300 | -800 | 400 | ps |
| DQ high-impedance time from CK, CK | tHZ(DQ) | - | 250 | - | 300 | - | 400 | ps |
| Data setup time to DQS, DQS referenced to Vih(ac)Vil(ac) levels | tDS(base) | -10 | - | 25 | - | 75 | - | ps |
| Data hold time to DQS, DQS referenced to Vih(ac)Vil(ac) levels | tDH(base) | 65 | - | 100 | - | 150 | - | ps |

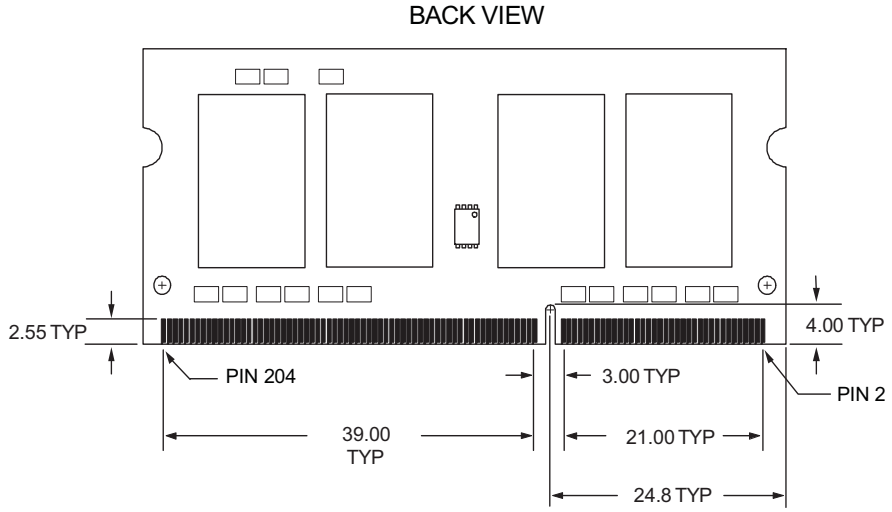
| AC TIMING PARAMETERS & SPECIFICATIONS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | DDR3-1333 | | DDR3-1066 | | DDR3-800 | | Unit |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **Data Strobe Timing** | | | | | | | | |
| DQS, DQS READ Preamble | tRPRE | 0.9 | - | 0.9 | - | 0.9 | - | tCK |
| DQS, DQS differential READ Postamble | tRPST | 0.3 | - | 0.3 | - | 0.3 | - | tCK |
| DQS, DQS output high time | tQSH | 0.4 | - | 0.38 | - | 0.38 | - | tCK(avg) |
| DQS, DQS output low time | tQSL | 0.4 | - | 0.38 | - | 0.38 | - | tCK(avg) |
| DQS, DQS WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | tCK |
| DQS, DQS WRITE Postamble | tWPST | 0.3 | - | 0.3 | - | 0.3 | - | tCK |
| DQS, DQS rising edge output access time from rising CK, CK | tDQSCK | -255 | 255 | -300 | 300 | -400 | 400 | ps |
| DQS, DQS low-impedance time (Referenced from RL-1) | tLZ(DQS) | -500 | 250 | -600 | 300 | -800 | 400 | ps |
| DQS, DQS high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 250 | - | 300 | - | 400 | ps |
| DQS, DQS differential input low pulse width | tDQSL | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| DQS, DQS differential input high pulse width | tDQSH | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| DQS, DQS rising edge to CK, CK rising edge | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | tCK(avg) |
| DQS,DQS failing edge setup time to CK, CK rising edge | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | tCK(avg) |
| DQS,DQS failing edge hold time to CK, CK rising edge | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | tCK(avg) |
| **Command and Address Timing** | | | | | | | | |
| DLL locking time | tDLLK | 512 | - | 512 | - | 512 | - | nCK |
| Internal READ Command to PRECHARGE Command delay | tRTP | max (4tCK,7.5ns) | - | max (4tCK,7.5ns) | - | max (4tCK,7.5ns) | - | |
| Delay from start of internal write transaction to internal read command | tWTR | max (4tCK,7.5ns) | - | max (4tCK,7.5ns) | - | max (4tCK,7.5ns) | - | |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | ns |
| Mode Register Set command cycle time | tMRD | 4 | - | 4 | - | 4 | - | tCK(avg) |
| Mode Register Set command update delay | tMOD | max (12tCK,15ns) | - | max (12tCK,15ns) | - | max (12tCK,15ns) | - | |
| CAS# to CAS# command delay | tCCD | 4 | - | 4 | - | 4 | - | nCK |
| Auto precharge write recovery + precharge time | tDAL(min) | | | WR + roundup (tRP / tCK(AVG)) | | | | nCK |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | nCK |
| ACTIVE to PRECHARGE command period | tRAS | 36 | 70,000 | 37.5 | 70,000 | 37.5 | 70,000 | ns |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max (4tCK,6ns) | - | max (4tCK,7.5ns) | - | max (4tCK,10ns) | - | |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | max (4tCK,7.5ns) | - | max (4tCK,10ns) | - | max (4tCK,10ns) | - | |
| Four activate window for 1KB page size | tFAW | 30 | - | 37.5 | - | 40 | - | ns |
| Four activate window for 2KB page size | tFAW | 45 | - | 50 | - | 50 | - | ns |
| Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 65 | - | 125 | - | 200 | - | ps |
| Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels | tIH(base) | 140 | - | 200 | - | 275 | - | ps |

| AC TIMING PARAMETERS & SPECIFICATIONS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | DDR3-1333 | | DDR3-1066 | | DDR3-800 | | Unit |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **Refresh Timing** | | | | | | | | |
| 512Mb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 90 | - | 90 | - | 90 | - | ns |
| 1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 110 | - | 110 | - | 110 | - | ns |
| 2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 160 | - | 160 | - | 160 | - | ns |
| 4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 300 | - | 300 | - | 300 | - | ns |
| 8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 350 | - | 350 | - | 350 | - | ns |
| Average periodic refresh interval (0°C<= TCASE <= 85 °C) | tREFI | 7.8 | | 7.8 | | 7.8 | | us |
| Average periodic refresh interval (85°C<= TCASE <= 95 °C) | tREFI | 3.9 | | 3.9 | | 3.9 | | us |
| **Calibration Timing** | | | | | | | | |
| Power-up and RESET calibration time | tZQinitl | 512 | - | 512 | - | 512 | - | tCK |
| Normal operation Full calibration time | tZQoper | 256 | - | 256 | - | 256 | - | tCK |
| Normal operation Short calibration time | tZQCS | 64 | - | 64 | - | 64 | - | tCK |
| **Reset Timing** | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max(5tCK, tRFC + 10ns) | - | max(5tCK, tRFC + 10ns) | - | max(5tCK, tRFC + 10ns) | - | |
| **Self Refresh Timing** | | | | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | max(5tCK,tRFC + 10ns) | - | max(5tCK,tRFC + 10ns) | - | max(5tCK, tRFC + 10ns) | - | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | tCK |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCKE(min) + 1tCK | - | tCKE(min) + 1tCK | - | tCKE(min) + 1tCK | - | |
| Valid Clock Requirement after Self Refresh Entry (SRE) | tCKSRE | max(5tCK,10ns) | - | max(5tCK,10ns) | - | max(5tCK,10ns) | - | |
| Valid Clock Requirement before Self Refresh Exit (SRX) | tCKSRX | max(5tCK,10ns) | - | max(5tCK,10ns) | - | max(5tCK,10ns) | - | |
| **Power Down Timing** | | | | | | | | |
| Exit Power Down with DLL to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max (3tCK,6ns) | - | max (3tCK,7.5ns) | - | max (3tCK,7.5ns) | - | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | max (10tCK,24ns) | - | max (10tCK,24ns) | - | max (10tCK,24ns) | - | |
| CKE minimum pulse width | tCKE | max (3tCK,5.625ns) | - | max (3tCK,5.625ns) | - | max (3tCK,7.5ns) | - | |
| Command pass disable delay | tCPDED | 1 | - | 1 | - | 1 | - | nCK |

| AC TIMING PARAMETERS & SPECIFICATIONS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | DDR3-1333 | | DDR3-1066 | | DDR3-800 | | Unit |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Power Down Entry to Exit Timing | tPD | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCK |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 1 | - | 1 | - | nCK |
| Timing of PRE command to Power Down entry | tPRPDEN | 1 | - | 1 | - | 1 | - | nCK |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL + 4 +1 | - | RL + 4 +1 | - | RL + 4 +1 | - | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF) | tWRPDEN | WL + 4 +(tWR/ tCK) | - | WL + 4 +(tWR/ tCK) | - | WL + 4 +(tWR/ tCK) | - | nCK |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF) | tWRAPDEN | WL + 4 +WR +1 | - | WL + 4 +WR +1 | - | WL + 4 +WR +1 | - | nCK |
| Timing of WR command to Power Down entry (BL4MRS) | tWRPDEN | WL + 2 +(tWR/ tCK) | - | WL + 2 +(tWR/ tCK) | - | WL + 2 +(tWR/ tCK) | - | nCK |
| Timing of WRA command to Power Down entry (BL4MRS) | tWRAPDEN | WL +2 +WR +1 | - | WL +2 +WR +1 | - | WL +2 +WR +1 | - | nCK |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 1 | - | 1 | - | |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | tCK |
| **ODT Timing** | | | | | | | | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | 4 | - | 4 | - | nCK |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | 6 | - | 6 | - | nCK |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 1 | 9 | 1 | 9 | 1 | 9 | ns |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 1 | 9 | 1 | 9 | 1 | 9 | ns |
| ODT turn-on | tAON | -250 | 250 | -300 | 30 | -400 | 400 | ps |
| RTT_NOM and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) |
| **Write Leveling Timing** | | | | | | | | |
| First DQS pulse rising edge after tDQSS margining mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | tCK |
| DQS/DQS delay after tDQS margining mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | tCK |
| Setup time for tDQSS latch | tWLS | 195 | - | 245 | - | 325 | - | ps |
| Hold time for tDQSS latch | tWLH | 195 | - | 245 | - | 325 | - | ps |
| Write leveling output delay | tWLO | 0 | 9 | 0 | 9 | 0 | 9 | ns |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | 0 | 2 | ns |

## Package Dimensions




Notes:

All dimensions are in millimeters with tolerance +/- 0.13mm unless otherwise specified.

## Revision History:

| Date | Rev. | Page | Changes |
|---|---|---|---|
| 02/18/09 | 1.0 | All | Release spec |
| 03/13/09 | 1.1 | 11 | Dimension Package update |
| | | | |
| | | | |