



Product Specifications

PART NO:

VL475S6553B-GAS

REV:

1.4

General Information

512MB 64Mx72 SDRAM PC133 ECC REGISTERED 144 PIN SODIMM

Description: The VL475S6553B is a 64Mx72 Synchronous Dynamic RAM high density memory module. This memory module consists of eighteen CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in TSOP-II 400 mil packages, two 14 bit Registered buffers in TSOP package, a zero delay buffer PLL in TSOP package, a and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Registered 8 byte SDRAM 144pin SODIMM
- High Speed - 133MHz CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ±0.3 V power supply
- 13/10/4 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial Presence Detect
- PCB height: **2000(mil)**, double sided component
- Gold (Au) contacts
- Lead-free/RoHS complaint

| Pin Name | Function |
|------------|----------------------------|
| A0-A12 | Address inputs |
| BA0, BA1 | Bank Select Address |
| DQ0-DQ63 | Data Input/Output |
| CB0-CB7 | Check bits |
| CLK0 | Clock Input |
| CKE0, CKE1 | Clock Enable Input |
| CS0#, CS1# | Chip Select Input |
| RAS# | Row Address Strobe |
| CAS# | Column Address Input |
| WE# | Write Enable |
| DQM0-DQM7 | Data input/output mask |
| VDD | Power Supply (3.3V) |
| VSS | Ground |
| *VREF | Power Supply for Reference |
| SDA | Serial Data Input/Output |
| SCL | SPD Clock Input |
| NC | No Connect |

* These pins are not used in this module.

Order Information:

VL 475S6553B-GA S X

DRAM DIE (Option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED
GA: PC133 @ CL3

VL: Lead-free/RoHS



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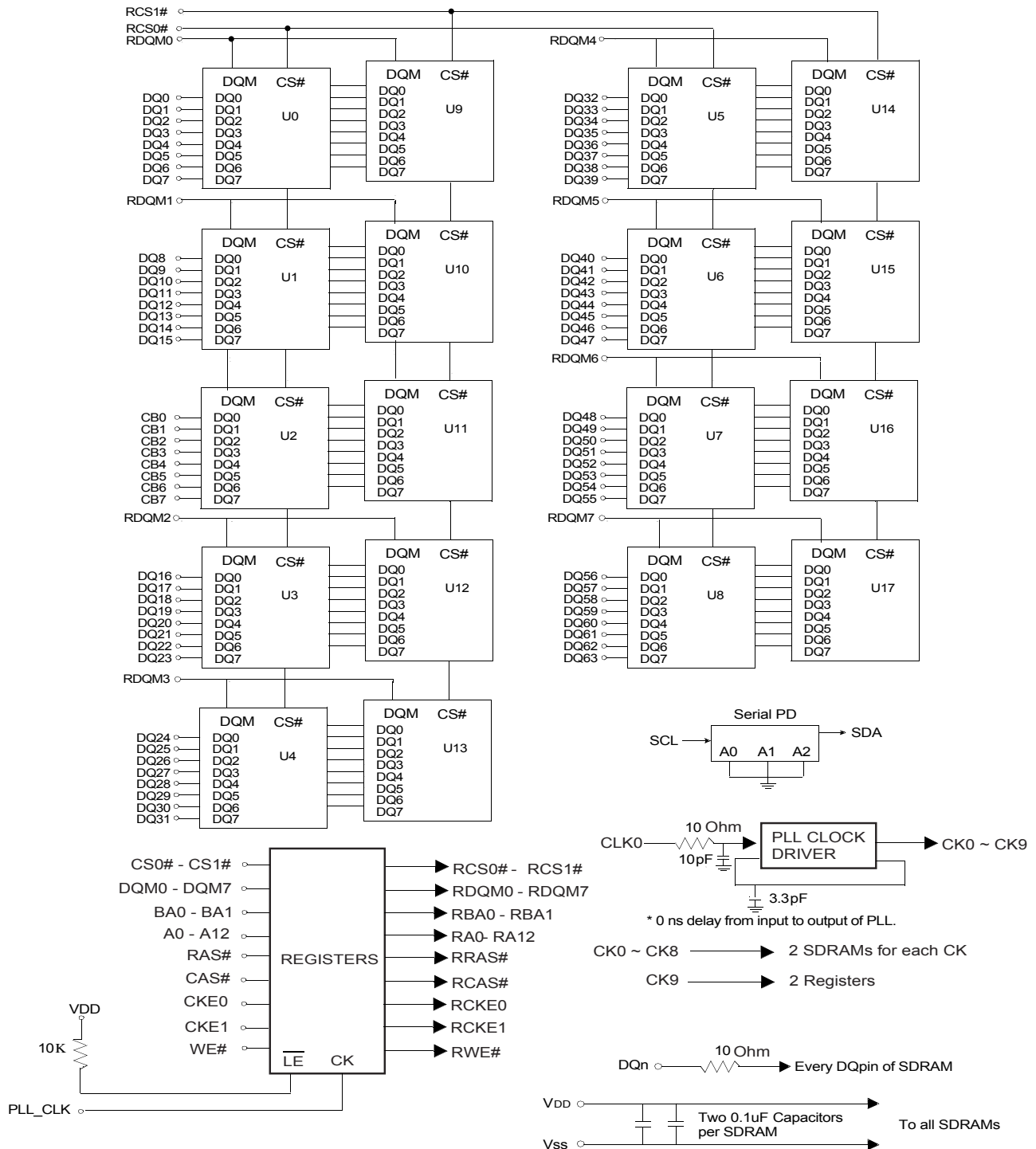
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Pin Configuration

| Pin Number | Front Side | Pin Number | Back Side | Pin Number | Front Side | Pin Number | Back Side |
|------------|------------|------------|-----------|------------|------------|------------|-----------|
| 1 | VSS | 2 | VSS | 73 | CS2#* | 74 | CS3#* |
| 3 | DQ0 | 4 | DQ32 | 75 | VSS | 76 | VSS |
| 5 | DQ1 | 6 | DQ33 | 77 | CB2 | 78 | CB6 |
| 7 | DQ2 | 8 | DQ34 | 79 | CB3 | 80 | CB7 |
| 9 | DQ3 | 10 | DQ35 | 81 | VDD | 82 | VDD |
| 11 | VDD | 12 | VDD | 83 | DQ16 | 84 | DQ48 |
| 13 | DQ4 | 14 | DQ36 | 85 | DQ17 | 86 | DQ49 |
| 15 | DQ5 | 16 | DQ37 | 87 | DQ18 | 88 | DQ50 |
| 17 | DQ6 | 18 | DQ38 | 89 | DQ19 | 90 | DQ51 |
| 19 | DQ7 | 20 | DQ39 | 91 | VSS | 92 | VSS |
| 21 | VSS | 22 | VSS | 93 | DQ20 | 94 | DQ52 |
| 23 | DQM0 | 24 | DQM4 | 95` | DQ21 | 96 | DQ53 |
| 25 | DQM1 | 26 | DQM5 | 97 | DQ22 | 98 | DQ54 |
| 27 | VDD | 28 | VDD | 99 | DQ23 | 100 | DQ55 |
| 29 | A0 | 30 | A3 | 101 | VDD | 102 | VDD |
| 31 | A1 | 32 | A4 | 103 | A6 | 104 | A7 |
| 33 | A2 | 34 | A5 | 105 | A8 | 106 | BA0 |
| 35 | VSS | 36 | VSS | 107 | VSS | 108 | VSS |
| 37 | DQ8 | 38 | DQ40 | 109 | A9 | 110 | BA1 |
| 39 | DQ9 | 40 | DQ41 | 111 | A10/AP | 112 | A11 |
| 41 | DQ10 | 42 | DQ42 | 113 | VDD | 114 | VDD |
| 43 | DQ11 | 44 | DQ43 | 115 | DQM2 | 116 | DQM6 |
| 45 | VDD | 46 | VDD | 117 | DQM3 | 118 | DQM7 |
| 47 | DQ12 | 48 | DQ44 | 119 | VSS | 120 | VSS |
| 49 | DQ13 | 50 | DQ45 | 121 | DQ24 | 122 | DQ56 |
| 51 | DQ14 | 52 | DQ46 | 123 | DQ25 | 124 | DQ57 |
| 53 | DQ15 | 54 | DQ47 | 125 | DQ26 | 126 | DQ58 |
| 55 | VSS | 56 | VSS | 127 | DQ27 | 128 | DQ59 |
| 57 | CB0 | 58 | CB4 | 129 | VDD | 130 | VDD |
| 59 | CB1 | 60 | CB5 | 131 | DQ28 | 132 | DQ60 |
| 61 | CLK0 | 62 | CKE0 | 133 | DQ29 | 134 | DQ61 |
| 63 | VDD | 64 | VDD | 135 | DQ30 | 136 | DQ62 |
| 65 | RAS# | 66 | CAS# | 137 | DQ31 | 138 | DQ63 |
| 67 | WE# | 68 | CKE1 | 139 | VSS | 140 | VSS |
| 69 | CS0# | 70 | A12 | 141 | SDA | 142 | SCL |
| 71 | CS1# | 72 | NC | 143 | VDD | 144 | VDD |

* These pins are not used in this module

Functional Block Diagram





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PART NO:

VL475S6553B-GAS

REV:

1.4

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------------------------------|------------|------|
| Voltage on any pin relative to V _{SS} | V _{IN} , V _{OUT} | -1.0 ~ 4.6 | V |
| Voltage on V _{DD} supply relative to V _{SS} | V _{DD} , V _{DDQ} | -1.0 ~ 4.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Power dissipation | P _D | 18 | W |
| Short circuit current | I _{OS} | 50 | mA |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A = 0°C to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--------------------------------|------------------------------------|------|-----|-----------------------|------|------------------------|
| Supply voltage | V _{DD} , V _{DDQ} | 3.0 | 3.3 | 3.6 | V | |
| Input high voltage | V _{IH} | 2.0 | 3.0 | V _{DDQ} +0.3 | V | 1 |
| Input low voltage | V _{IL} | -0.3 | 0 | 0.8 | V | 2 |
| Output high voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -2mA |
| Output low voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA |
| Input leakage current (Inputs) | I _{IL} | -8 | - | 8 | µA | 3 |

Notes: 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = 2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Capacitance (T_A = 25°C, f = 1MHz, V_{DD} = 3.3V)

| Parameter | Symbol | Min | Max | Unit |
|---|------------------|-----|-----|------|
| Input capacitance (A0 ~ A12, BA0 ~ BA1) | C _{IN1} | - | 15 | pF |
| Input capacitance (RAS#, CAS#, WE#) | C _{IN2} | - | 15 | pF |
| Input capacitance (CKE0, CKE1) | C _{IN3} | - | 15 | pF |
| Input capacitance (CLK0) | C _{IN4} | - | 12 | pF |
| Input capacitance (CS0#, CS1#) | C _{IN5} | - | 12 | pF |
| Input capacitance (DQM0 ~ DQM7) | C _{IN6} | - | 12 | pF |
| Data input/output capacitance (DQ0 ~ DQ63), (CB0 ~ CB7) | C _{OUT} | - | 12 | pF |



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VL475S6553B-GAS

REV:

1.4

| DC Characteristics (Recommended operation condition unless otherwise noted, TA = 0°C to +70°C) | | | | | |
|--|--------------------|--|---------|------|------|
| Parameter | Symbol | Test Condon | Version | Unit | Note |
| | | | -GA | | |
| Operating current (One bank active) | I _{CC1} | Burst length = 1 trc >= trc(min) I _{OL} = 0 mA | 1445 | mA | 1 |
| Precharge standby current in power-down mode | I _{CC2P} | CKE <= V _{IL} (max), tcc = 10ns | 390 | mA | |
| | I _{CC2PS} | CKE & CLK <= V _{IL} (max), tcc = ∞ | 40 | mA | |
| Precharge standby current in non power-down mode | I _{CC2N} | CKE >= V _H (min), CS# >= V _H (min), tcc = 10ns Input signals are changed one time during 20ns | 710 | mA | |
| | I _{CC2NS} | CKE >= V _H (min), CLK <= V _{IL} (max), tcc = ∞ Input signals are stable | 185 | mA | |
| Active standby current in power- down mode | I _{CC3P} | CKE <= V _{IL} (max), tcc = 10ns | 460 | mA | |
| | I _{CC3PS} | CKE & CLK <= V _{IL} (max), tcc = ∞ | 110 | mA | |
| Active standby current in non power-down mode (One bank active) | I _{CC3N} | CKE >= V _H (min), CS# >= V _H (min), tcc = 10ns Input signals are changed one time during 20ns | 800 | mA | |
| | I _{CC3NS} | CKE >= V _H (min), CLK <= V _{IL} (max), tcc = ∞ Input signals are stable | 455 | mA | |
| Operating current (Burst mode) | I _{CC4} | I _{OL} = 0 mA Page burst 2 Banks actived tccD = 2CLKs | 1625 | mA | 1 |
| Refresh current | I _{CC5} | trc >= trc(min) | 2345 | mA | 2 |
| Self refresh current | I _{CC6} | CKE <= 0.2V | 405 | mA | |
| Note: 1. Measured with outputs open. 2.Refresh period is 64ms. | | | | | |

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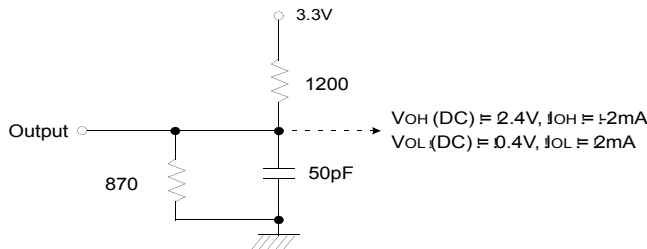
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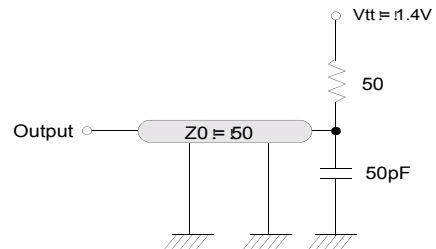
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AC Operating Test Conditions (VDD = 3.3V, TA = 0°C to +70°C)

| Parameter | Value | Unit |
|---|-------------|------|
| AC input levels (V _H /V _L) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig.2 | |



(Fig. 1) DC output load circuit!



(Fig. 2) AC output load circuit!

Operating AC Parameter

| Parameter | Symbol | Version | Unit | Note |
|--|------------------------|-------------------------|------|------|
| | | -GA | | |
| Row active to row active delay | t _{RRD} (min) | 15 | ns | 1 |
| RAS# to CAS# delay | t _{RCD} (min) | 20 | ns | 1 |
| Row precharge time | t _{RP} (min) | 20 | ns | 1 |
| Row active time | t _{RAS} (min) | 45 | ns | 1 |
| | t _{RAS} (max) | 100 | us | |
| Row cycle time | t _{RC} (min) | 65 | ns | 1 |
| Last data in to row precharge | t _{RDL} (min) | 2 | CLK | 2 |
| Last data in to Active delay | t _{DAL} (min) | 2 CLK + t _{RP} | - | |
| Last data in to new col. address delay | t _{CDL} (min) | 1 | CLK | 2 |
| Last data in to burst stop | t _{BDL} (min) | 1 | CLK | 2 |
| Col. address to col. address delay | t _{CCD} (min) | 1 | CLK | 3 |
| Number of valid output data | CAS Latency = 3 | 2 | CLK | 4 |

- Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.



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VL475S6553B-GAS

REV:

1.4

Operating AC Parameter

| Parameter | Symbol | -GA | | Unit | Note | |
|---------------------------|-----------------|------|-----|------|------|-----|
| | | Min | Max | | | |
| CLK cycle time | CAS latency = 3 | tCC | 7.5 | 1000 | ns | 1 |
| | CAS latency = 2 | | - | | | |
| CLK to valid output delay | CAS latency = 3 | tSAC | | 5.4 | ns | 1,2 |
| | CAS latency = 2 | | | - | | |
| Output data hold time | CAS latency = 3 | tOH | 3 | | ns | 2 |
| | CAS latency = 2 | | | - | | |
| CLK high pulse width | | tCH | 2.5 | | ns | 3 |
| CLK low pulse width | | tCL | 2.5 | | ns | 3 |
| Input setup time | | tSS | 1.5 | | ns | 3 |
| Input hold time | | tSH | 0.8 | | ns | 3 |
| CLK to output in Low-Z | | tSLZ | 1 | | ns | 2 |
| CLK to output in Hi-z | CAS latency = 3 | tSHZ | | 5.4 | ns | |
| | CAS latency = 2 | | | - | | |

Notes: 1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 3. Assumed input rise and fall time (tr & tf) = 1ns.
 if tr & tf is longer than 1ns, transient timecompensation should be considered,
 i.e. $[(tr + tf)/2-1]$ ns should be added to the parameter.

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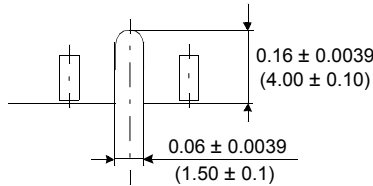
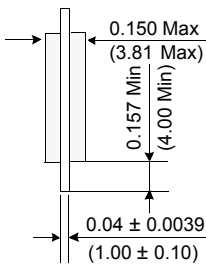
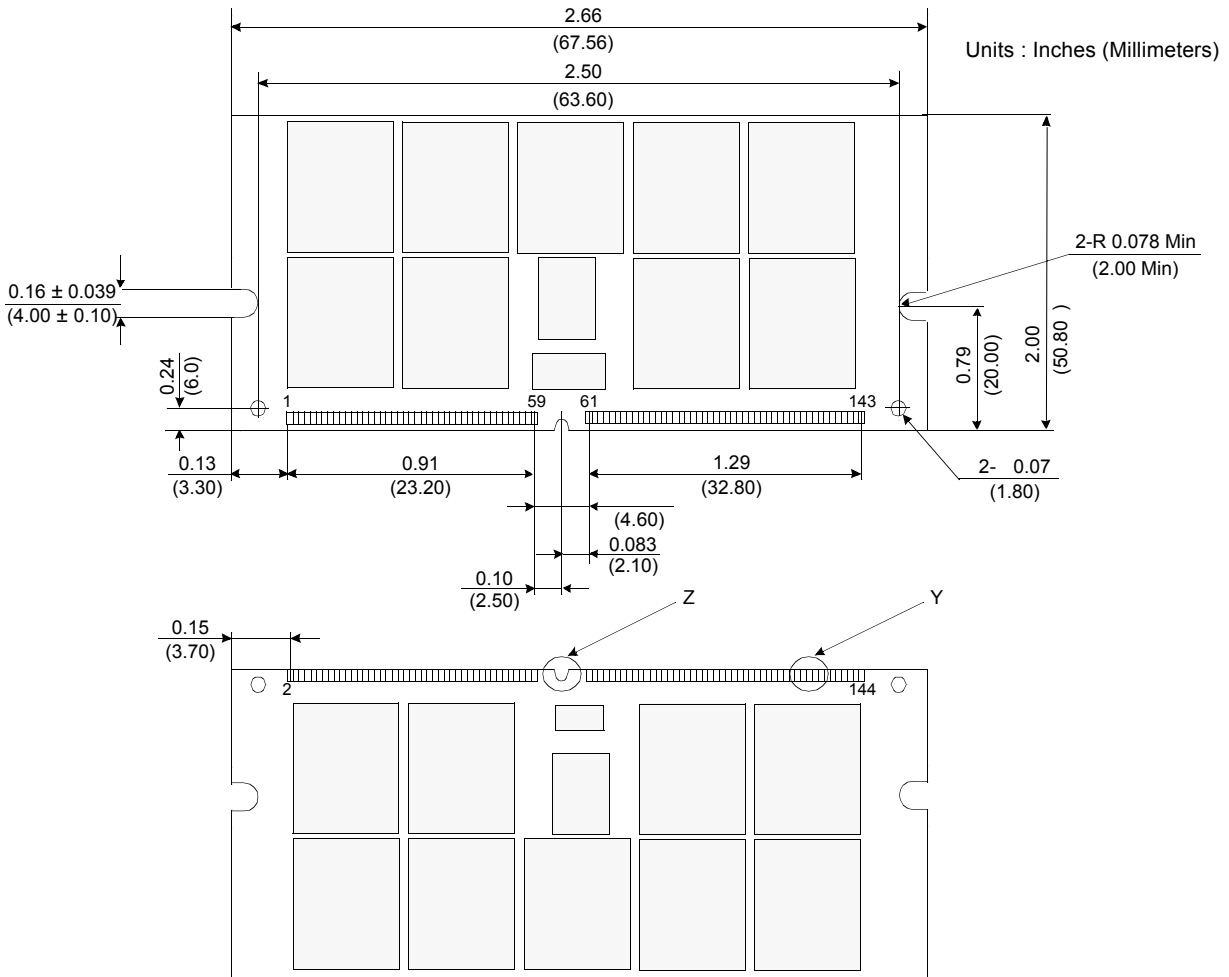
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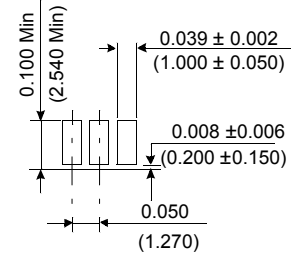
REV:

1.4

Package Dimensions



Detail Z



Detail Y

Tolerance: + .006 (.15) unless otherwise specified

Revision History:

| Date | Rev. | Page | Changes |
|------------|------|------|------------------|
| 09/23/2010 | 1.4 | All | Update datasheet |
| | | | |