



Product Specification

1GB 128MX72 ECC SDRAM PC100/PC133 SODIMM

Revision: 1.2

General Information

VL474S2858B-IAS

1GB 128Mx72 ECC SDRAM PC133 SODIMM W/PLL

Description: The VL474S2858B is a 128M x 72 Synchronous Dynamic RAM high density memory module. This memory module consists of nine stacked CMOS 128Mx8 bits SDRAM TSOP-II 400mil packages, and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin Small-outline Dual In-line Memory Module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Unbuffered 8 byte SDRAM 144pin DIMM
- High Speed - 133MHz CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ±0.3 V power supply
- 13/11/2 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial presence Detect
- Gold (Au) contacts
- Lead-free/RoHS compliant
- PCB height: **1250 (mil)**, single sided component
- Industrial temperature: -40°C to + 85°C

Pin Names:

Pin Name	Function
A0-A12	Address Input
BA0,BA1	Select Bank
DQ0-DQ63	Data Input/output
CB0-CB7	Check bits for ECC
CLK0	Clock Input
CKE0, CKE1	Clock Enable Input
/CS0, /CS1	Chip Select Input
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQM0-7	DQM
SCL	Serial Clock
SDA	Serial Data I/O
V _{DD}	Power supply (3.3V)
V _{SS}	Ground
NC	No connection
DU	Don't Use

Order Information:

VL470S2858B-IA S X

DRAM DIE (option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED
IA: PC133 @ CL3
(I: Industrial grade)

VL : Lead-free/RoHS



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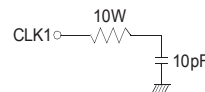
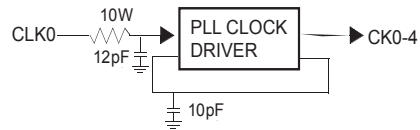
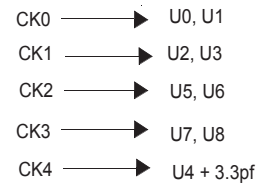
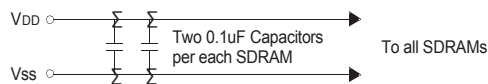
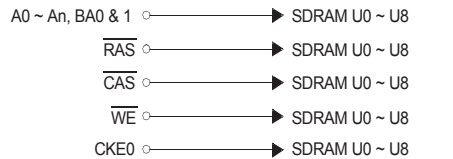
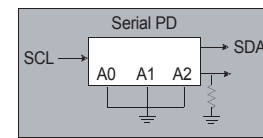
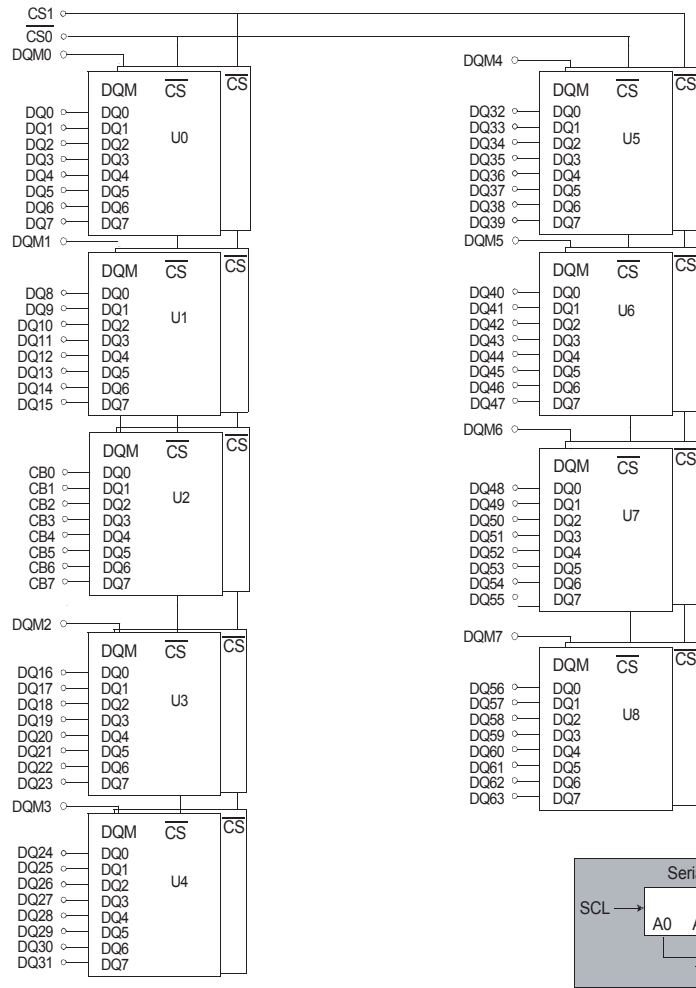
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Pin Configuration

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Pin Number	Front Side	Pin Number	Back Side	Pin Number	Front Side	Pin Number	Back Side
1	VSS	2	VSS	73	DU	74	*CLK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	CB2	78	CB6
7	DQ2	8	DQ34	79	CB3	80	CB7
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10/AP	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	VDD	46	VDD	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	CB0	58	CB4	129	VDD	130	VDD
59	CB1	60	CB5	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	/RAS	66	/CAS	137	DQ31	138	DQ63
67	/WE	68	CKE1	139	VSS	140	VSS
69	/CS0	70	A12	141	SDA	142	SCL
71	/CS1	72	NC	143	VDD	144	VDD

Functional Block Diagram

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Absolute Maximum Ratings

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Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Ambient operating temperature	T _A	-40 ~ +85	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A = -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

Capacitance

(T_A=25, f=1MHz, V_{DD}=3.3V)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₂)	C _{IN1}	50	95	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	50	95	pF
Input capacitance (CKE ₀ , CKE ₁)	C _{IN3}	25	50	pF
Input capacitance (CLK ₀)	C _{IN4}	15	18	pF
Input capacitance (CS ₀ , CS ₁)	C _{IN5}	25	50	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	5	10	pF
Input capacitance (BA ₀ ~ BA ₁)	C _{IN7}	50	95	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	-	16	pF
Data input/output capacitance (CB ₀ ~ CB ₇)	C _{OUT1}	-	16	pF



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DC Characteristics

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(Recommended operating condition unless otherwise noted, TA = -40 to +85°C)

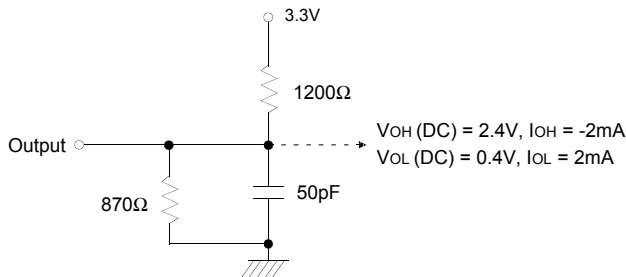
Parameter	Symbol	Test Condition	Value	Unit	Note
			-IA		
Operating current (One bank active)	I _{CC1}	Burst length =1 t _{RC} ≥ t _{RC(min)} I _O = 0 mA	1080	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL(max)} , t _{CC} = 10ns	36	mA	3
	I _{CC2PS}	CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞	36		
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH(min)} , $\overline{CS} \geq V_{IH(min)}$, t _{CC} = 10ns Input signals are changed one time during 20ns	360	mA	3
	I _{CC2NS}	CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable	180		
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL(max)} , t _{CC} = 10ns	108	mA	3
	I _{CC3PS}	CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞	108		
Active standby current in non power-down mode	I _{CC3N}	CKE ≥ V _{IH(min)} , $\overline{CS} \geq V_{IH(min)}$, t _{CC} = 10ns Input signals are changed one time during 20ns	540	mA	3
	I _{CC3NS}	CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable	450		
Operating current (Burst mode)	I _{CC4}	I _O = 0mA Page Burst 4 Banks activated t _{CCD} =2CLK	1260	mA	1
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(min)}	2070	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	54	mA	3

- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 3 Drive ICs.

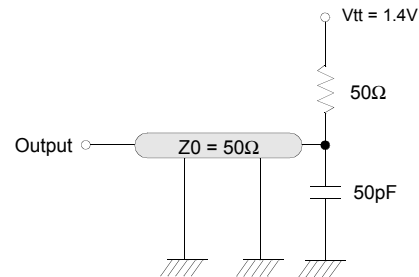
AC Operating Test Conditions ($V_{dd}=3.3V, 0 - 70C$)

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Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Operating AC Parameter

Parameter	Symbol	Version				Unit	Note
		-I7	-IA	-IH	-IL		
Row active to row active delay	$t_{RRD}(\min)$	20	20	15	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	20	15	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	20	15	20	ns	1
Row active time	$t_{RAS}(\min)$	50	50	45	45	ns	1
	$t_{RAS}(\max)$	100				us	
Row cycle time	$t_{RC}(\min)$	70	70	60	65	ns	1
Last data in to row precharge	$t_{RD}(\min)$	2				CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + t_{RP}				-	
Last data in to new col. address delay	$t_{CDL}(\min)$	1				CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1				CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1				CLK	3
Number of valid output data	CAS latency=3	2				ea	4
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.



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Operating AC Parameters

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REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

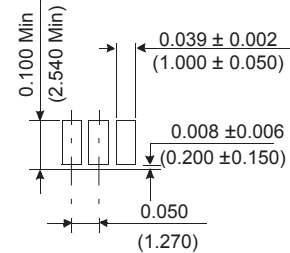
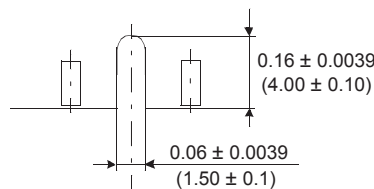
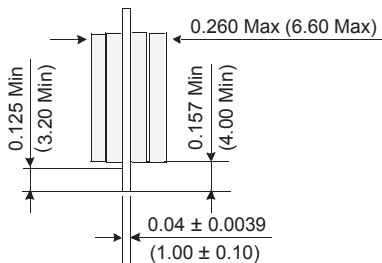
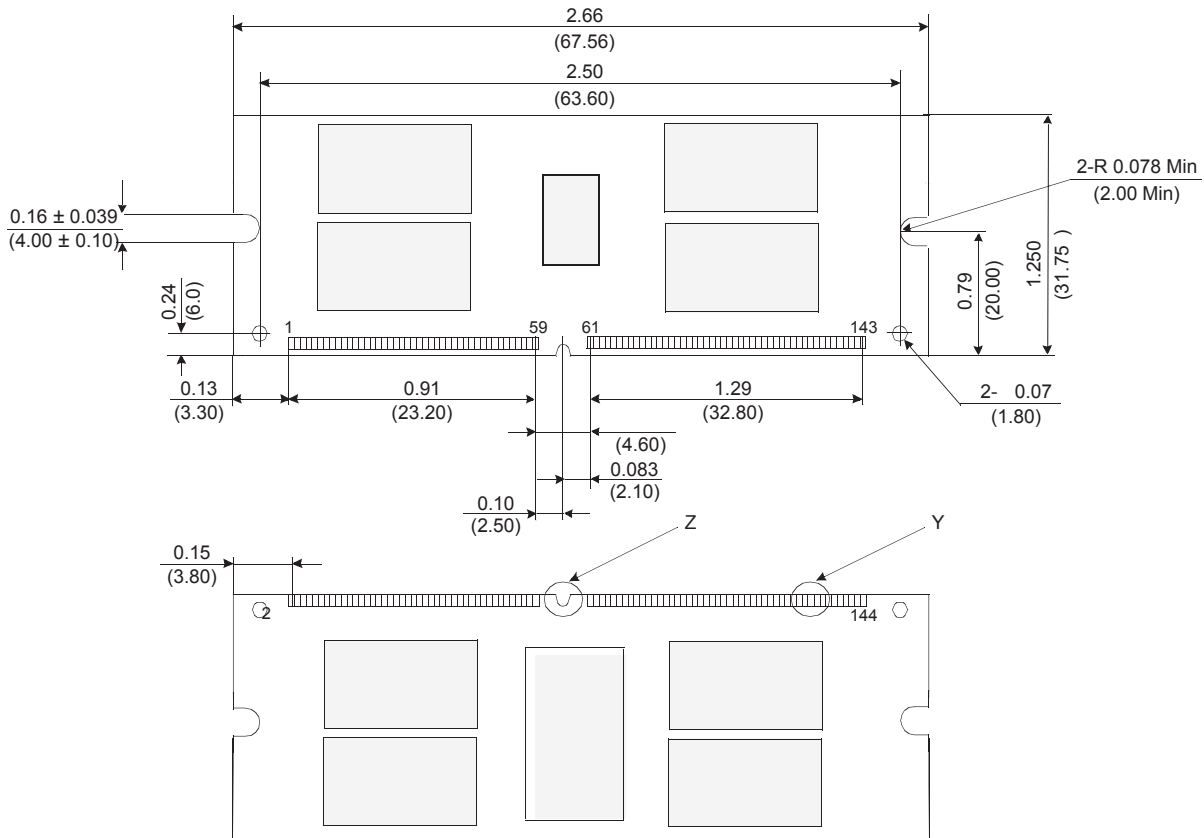
Parameter		Symbol	-I7		-IA		-IH		-IL		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		7.5		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		5.4		5.4		6		6	ns	1,2
	CAS latency=2			5.4		6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	2.5		2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		2.5		3		3		ns	3
Input setup time		tSS	1.5		1.5		2		2		ns	3
Input hold time		tSH	0.8		0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		5.4		6		6	ns	
	CAS latency=2			5.4		6		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

Package Dimensions

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Units : Inches (Millimeters)



Detail Z

Detail Y

Revision History:

Date	Rev.	Page	Changes
09/23/2010	1.2	All	Update datasheet