

Product Specifications		
PART NO.:	VL470T2863E-E6S	REV: 1.0

General Information

1GB 128Mx64 DDR2 SDRAM NON-ECC UNBUFFERED SODIMM 200-PIN

Description

The VL470T2863E is a 128Mx64 DDR2 SDRAM high density SODIMM. This memory module consists of eight CMOS 128Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 200-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

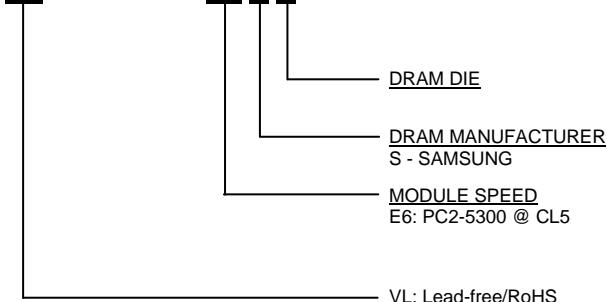
- 200-pin, small-outline dual in-line memory module (SODIMM)
- JEDEC pin out
- Fast data transfer rate: PC2-5300
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 5 (DDR2-667)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 18.29mm (0.720"), double sided components

Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes
DQS0#~DQS7#	Data Strobes Complement
ODT0	On-die Termination Control
CK0, CK0#, CK1, CK1#	Clock Input
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
DM0~DM7	Data Masks
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

Order Information:

VL470T2863A-E6 S X





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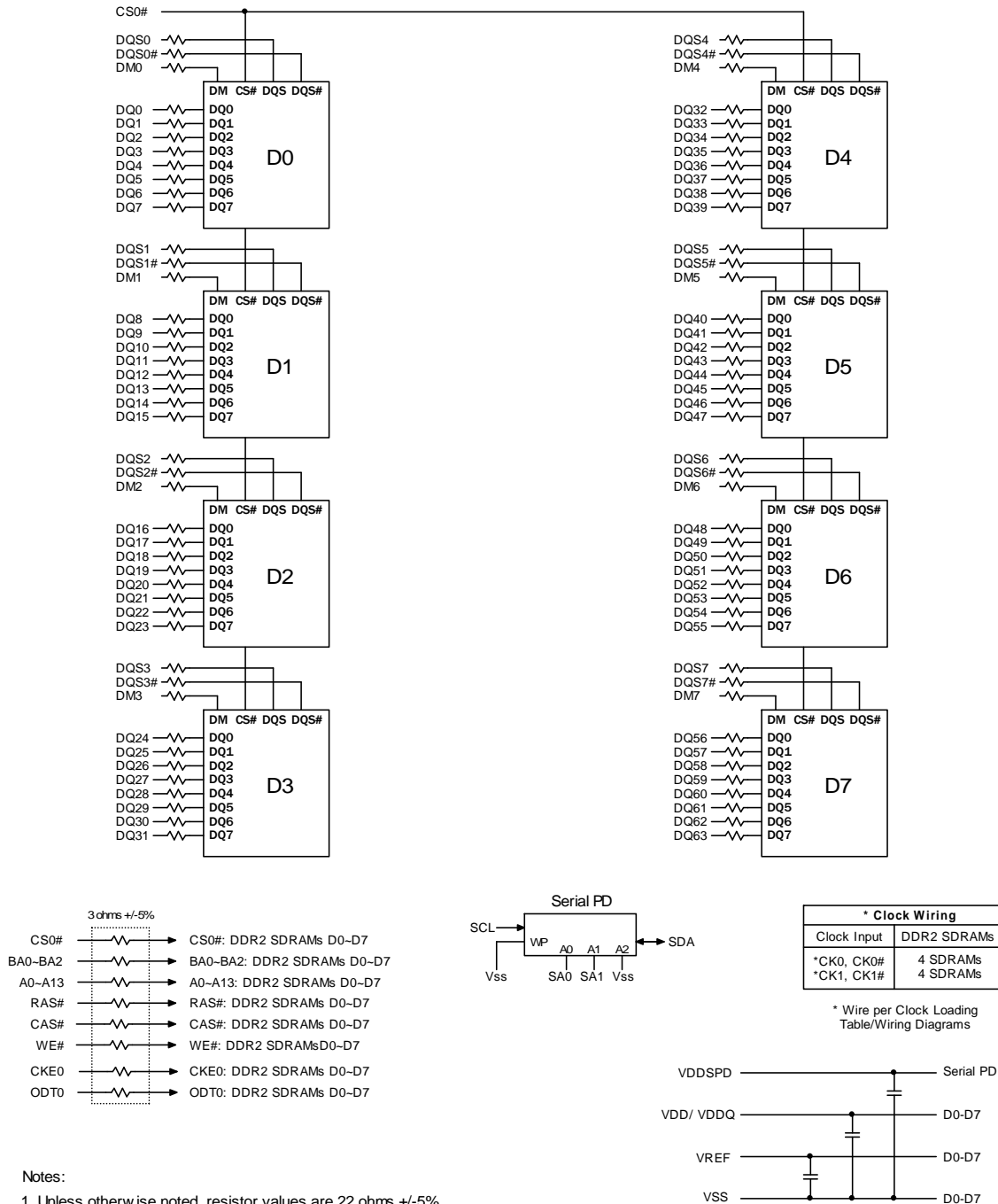
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Pin Configuration

200-PIN DDR2 SODIMM FRONT								200-PIN DDR2 SODIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	51	DQS2	101	A1	151	DQ42	2	VSS	52	DM2	102	A0	152	DQ46
3	VSS	53	VSS	103	VDD	153	DQ43	4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS	6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	VSS	58	DQ23	108	RAS#	158	DQ52
9	VSS	59	VSS	109	WE#	159	DQ49	10	DM0	60	VSS	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	VSS	12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	OTD0	164	CK1
15	VSS	65	VSS	115	CS1# *	165	VSS	16	DQ7	66	VSS	116	A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	VSS	68	DQS3#	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1 *	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS	22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS	28	VSS	78	VSS	128	VSS	178	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1 *	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS	34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	NC	135	DQ34	185	DM7	36	DQ14	86	A14*	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	VSS	38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58	40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59	42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS	44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	VSS
47	VSS	97	A5	147	DM5	197	SCL	48	VSS	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	VSS	199	VDDSPD	50	NC	100	A2	150	VSS	200	SA1

*: These pins are not used on this module.

Function Block Diagram



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Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit	
VDD	Voltage on VDD pin relative to VSS	-1.0	2.3	V	
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5	2.3	V	
VDDL	Voltage on VDDL pin relative to VSS	-0.5	2.3	V	
VIN, VOUT	Voltage on any pin relative to VSS	-0.5	2.3	V	
TSTG	Storage temperature	-55	100	°C	
IL	Input leakage current; Any input $0V < V_{IN} < V_{DD}$; VREF input $0V < V_{IN} < 0.95V$; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-40	40	uA
		CS#, CKE, ODT	-40	40	uA
		CK, CK#	-40	40	uA
		DM	-5	5	uA
IOZ	Output leakage current; $0V < V_{OUT} < V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level	-16	16	uA	

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2
VTT	I/O termination voltage	$V_{REF} - 0.04$	VREF	$V_{REF} + 0.04$	V	3

Note:

1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

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Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 to 95	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 to +85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TOPER <= 95°C.				

Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.200	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	12	20	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	12	20	pF
Input capacitance (CK0, CK0#, CK1, CK1#)	CIN3	8	12	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	6.5	7.5	pF

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IDD Specification

Condition	Symbol	-E6	Unit
Operating one bank active-pre-charge current; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	560	mA
Operating one bank active-read-pre-charge current; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1*	640	mA
Pre-charge power-down current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P**	120	mA
Pre-charge quiet standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	240	mA
Pre-charge standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	IDD2N**	280	mA
Active power-down current; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	Fast PDN Exit MRS(12) = 0	280
		Slow PDN Exit MRS(12) = 1	144
Active standby current; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RP} = t_{RP(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	400	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W*	840	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	960	mA
Burst refresh current; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	1120	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	120
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7*	1840	mA

Notes: IDD specification is based on Samsung Q-die components.

*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.



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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-667 (-E6)		Unit	
		MIN	MAX		
Clock Timing					
Clock Cycle Time	CL5	$t_{CK(5)}$	3000	8000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	$t_{CK(avg)}$
CK low-level width		$t_{CL(avg)}$	0.48	0.52	$t_{CK(avg)}$
Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})	-	ps
Clock jitter		t_{JIT}	-125	125	ps
Data Timing					
DQ output access time from CK/CK#		t_{AC}	-450	450	ps
Data-out high impedance window from CK/CK#		t_{HZ}	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		t_{LZ}	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		t_{DS}	100	-	ps
DQ and DM input hold time relative to DQS		t_{DH}	175	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35	-	$t_{CK(avg)}$
Data hold skew factor		t_{QHS}	-	340	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	$t_{HP} - t_{QHS}$	-	ps
Data valid output window (DVW)		t_{DVW}	$t_{QH} - t_{DQSQ}$	-	ns
Data Strobe Timing					
DQS input high pulse width		t_{DQSH}	0.35	-	$t_{CK(avg)}$
DQS input low pulse width		t_{DQSL}	0.35	-	$t_{CK(avg)}$
DQS output access time from CK/CK#		t_{DQSCK}	-400	400	ps
DQS failing edge to CK rising-setup time		t_{DSS}	0.2	-	$t_{CK(avg)}$
DQS failing edge from CK rising-hold time		t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	240	ps
DQS read preamble		t_{RPRE}	0.9	1.1	$t_{CK(avg)}$
DQS read preamble		t_{RPST}	0.4	0.6	$t_{CK(avg)}$
DQS read preamble setup time		t_{WPRES}	0	-	ps
DQS read preamble		t_{WPRE}	0.35	-	$t_{CK(avg)}$
DQS read preamble		t_{WPST}	0.4	0.6	$t_{CK(avg)}$
Write command to first DQS latching transition		t_{DQSS}	-0.25	0.25	$t_{CK(avg)}$

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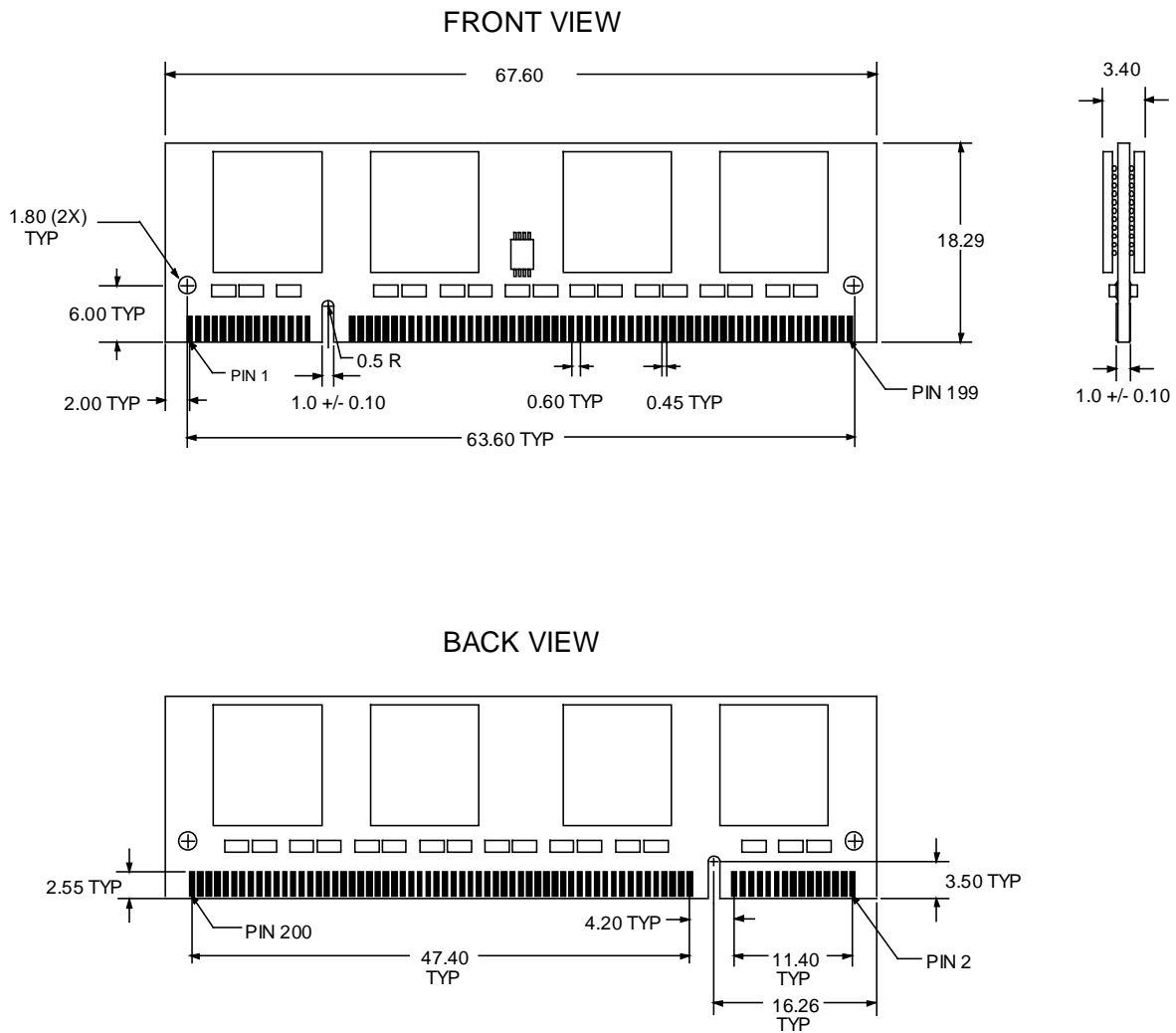
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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-667 (-E6)		Unit
		MIN	MAX	
Command and Address Timing				
Address and control input pulse width for each input	t_{IPW}	0.6	-	$t_{CK(AVG)}$
Address and control input setup time	t_{IS}	200	-	ps
Address and control input hold time	t_{IH}	275	-	ps
CAS# to CAS# command delay	t_{CCD}	2	-	ps
ACTIVE to ACTIVE (same bank) command	t_{RC}	60	-	ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	ns
Four Bank Activate period	t_{FAW}	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70000	ns
Internal READ to precharge Command delay	t_{RTP}	7.5	-	ns
Write recovery time	t_{WR}	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} - t_{RP}$	-	ns
Internal WRITE to READ Command delay	t_{WTR}	7.5	-	ns
PRECHARGE command period	t_{RP}	15	-	ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	-	ns
Self Refresh				
Refresh to Active or Refresh to Refresh command interval	t_{RFC}	127.5	70000	ns
Average periodic Refresh interval	t_{REFI}	-	7.8	us
Exit Self Refresh to non-READ command	t_{XSNR}	$t_{RFC} + 10$	-	ns
Exit Self Refresh to READ	t_{XSRD}	200	-	t_{CK}
Exit Self Refresh timing reference	t_{ISXR}	t_{IS}	-	ps
ODT				
ODT turn-on delay	t_{AOND}	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)} + 700$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	ps
ODT turn-on(power-down mode)	t_{AONPD}	$t_{AC(MIN)} + 2000$	$2 * t_{CK(AVG)} + t_{AC(MAX)} + 1000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{AC(MIN)} + 2000$	$2.5 * t_{CK(AVG)} + t_{AC(MAX)} + 1000$	ps
ODT to power-down entry latency	t_{ANPD}	3	-	t_{CK}
ODT power-down exit latency	t_{AXPD}	8	-	t_{CK}
Power Down				
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	t_{CK}
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7 - AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	t_{CK}

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Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.



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Revision History:

Date	Rev.	Page	Changes
04/08/2010	1.0	All	Spec release