



Product Specifications

PART NO:

VL470L2925F-B3S

REV: 1.0

General Information

1GB 128MX64 DDR SDRAM UNBUFFERED 200 PIN SODIMM

Description The VL470L2925F is a 128Mx64 Double Data Rate SDRAM high density unbuffered SODIMM. This memory module consists of sixteen CMOS 64Mx8 bit with 4 banks DDR Synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 200-pin dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR SDRAM.

Features

- Power supply: VDD: 2.5V +/- 0.2V, VDDQ: 2.5V +/- 0.2V
- Two data transfers per clock cycle
- Bi-directional data strobe (DQS)
- Differential clock inputs (CK and CK#)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency: DDR333(2.5 clock)
- Programmable burst; length (2, 4, 8)
- Programmable burst (sequential & interleave)
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- PCB: Height 26.67mm (1.050"), double sided components

| Pin Name | Function |
|-----------------------|------------------------------|
| A0~A12 | Address Inputs |
| BA0, BA1 | Bank Select Address |
| DQ0~DQ63 | Data Inputs/Outputs |
| DQS0~DQS7 | Data Strobe Inputs/Outputs |
| CK0, CK0# ~ CK1, CK1# | Clock Inputs |
| CKE0~CKE1 | Clock Enable Inputs |
| CS0#~CS1# | Chip Select Inputs |
| RAS# | Row Address Strobes |
| CAS# | Column Address Inputs |
| WE# | Write Enable |
| DM0~DM7 | Data Masks |
| VDD | Power Supply |
| VDDQ | Power Supply for DQS |
| VSS | Ground |
| VREF | Power Supply for Reference |
| VDDSPD | SPD Power Supply (2.3V-3.6V) |
| SDA | Serial Data Input/Output |
| SCL | SPD Clock Input |
| SA0~SA2 | SPD Address |
| NC | No Connect |

Order Information

VL470L2925F-B3 S X

DRAM DIE (Option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED
B3: PC2700 @ CL2.5

VL : Lead-free/RoHS



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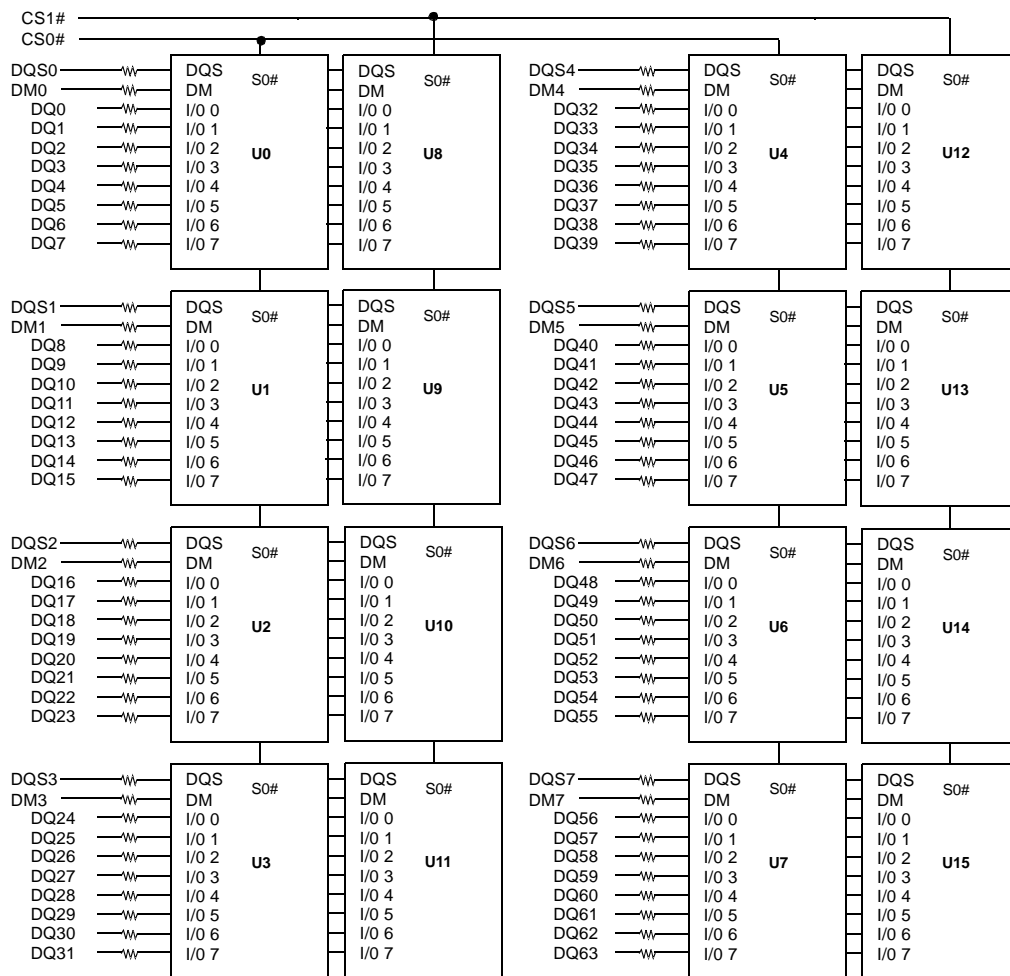
REV: 1.0

Pin Configuration

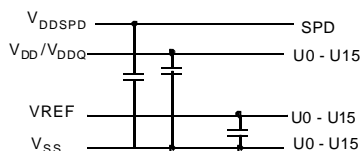
| 200-PIN DDR SODIMM FRONT | | | | | | | | 200-PIN DDR SODIMM BACK | | | | | | | |
|--------------------------|------|-----|-------|-----|------|-----|--------|-------------------------|------|-----|------|-----|------|-----|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | | |
| 1 | VREF | 51 | VSS | 101 | A9 | 151 | DQ42 | 2 | VREF | 52 | VSS | 102 | A8 | 152 | DQ46 |
| 3 | VSS | 53 | DQ19 | 103 | VSS | 153 | DQ43 | 4 | VSS | 54 | DQ23 | 104 | VSS | 154 | DQ47 |
| 5 | DQ0 | 55 | DQ24 | 105 | A7 | 155 | VDD | 6 | DQ4 | 56 | DQ28 | 106 | A6 | 156 | VDD |
| 7 | DQ1 | 57 | VDD | 107 | A5 | 157 | VDD | 8 | DQ5 | 58 | VDD | 108 | A4 | 158 | CK1# |
| 9 | VDD | 59 | DQ25 | 109 | A3 | 159 | VSS | 10 | VDD | 60 | DQ29 | 110 | A2 | 160 | CK1 |
| 11 | DQS0 | 61 | DQS3 | 111 | A1 | 161 | VSS | 12 | DM0 | 62 | DM3 | 112 | A0 | 162 | VSS |
| 13 | DQ2 | 63 | VSS | 113 | VDD | 163 | DQ48 | 14 | DQ6 | 64 | VSS | 114 | VDD | 164 | DQ52 |
| 15 | VSS | 65 | DQ26 | 115 | A10 | 165 | DQ49 | 16 | VSS | 66 | DQ30 | 116 | BA1 | 166 | DQ53 |
| 17 | DQ3 | 67 | DQ27 | 117 | BA0 | 167 | VDD | 18 | DQ7 | 68 | DQ31 | 118 | RAS# | 168 | VDD |
| 19 | DQ8 | 69 | VDD | 119 | WE# | 169 | DQS6 | 20 | DQ12 | 70 | VDD | 120 | CAS# | 170 | DM6 |
| 21 | VDD | 71 | CB0* | 121 | CS0# | 171 | DQ50 | 22 | VDD | 72 | CB4* | 122 | CS1# | 172 | DQ54 |
| 23 | DQ9 | 73 | CB1* | 123 | NC | 173 | VSS | 24 | DQ13 | 74 | CB5* | 124 | NC | 174 | VSS |
| 25 | DQS1 | 75 | VSS | 125 | VSS | 175 | DQ51 | 26 | DM1 | 76 | VSS | 126 | VSS | 176 | DQ55 |
| 27 | VSS | 77 | DQS8* | 127 | DQ32 | 177 | DQ56 | 28 | VSS | 78 | DM8* | 128 | DQ36 | 178 | DQ60 |
| 29 | DQ10 | 79 | CB2* | 129 | DQ33 | 179 | VDD | 30 | DQ14 | 80 | CB6* | 130 | DQ37 | 180 | VDD |
| 31 | DQ11 | 81 | VDD | 131 | VDD | 181 | DQ57 | 32 | DQ15 | 82 | VDD | 132 | VDD | 182 | DQ61 |
| 33 | VDD | 83 | CB3* | 133 | DQS4 | 183 | DQS7 | 34 | VDD | 84 | CB7* | 134 | DM4 | 184 | DM7 |
| 35 | CK0 | 85 | NC | 135 | DQ34 | 185 | VSS | 36 | VDD | 86 | NC | 136 | DQ38 | 186 | VSS |
| 37 | CK0# | 87 | VSS | 137 | VSS | 187 | DQ58 | 38 | VSS | 88 | VSS | 138 | VSS | 188 | DQ62 |
| 39 | VSS | 89 | CK2* | 139 | DQ35 | 189 | DQ59 | 40 | VSS | 90 | VSS | 140 | DQ39 | 190 | DQ63 |
| 41 | DQ16 | 91 | CK2#* | 141 | DQ40 | 191 | VDD | 42 | DQ20 | 92 | VDD | 142 | DQ44 | 192 | VDD |
| 43 | DQ17 | 93 | VDD | 143 | VDD | 193 | SDA | 44 | DQ21 | 94 | VDD | 144 | VDD | 194 | SA0 |
| 45 | VDD | 95 | CKE1 | 145 | DQ41 | 195 | SCL | 46 | VDD | 96 | CKE0 | 146 | DQ45 | 196 | SA1 |
| 47 | DQS2 | 97 | NC | 147 | DQS5 | 197 | VDDSPD | 48 | DM2 | 98 | NC | 148 | DM5 | 198 | SA2 |
| 49 | DQ18 | 99 | A12 | 149 | VSS | 199 | NC | 50 | DQ22 | 100 | A11 | 150 | VSS | 200 | NC |

Note: *: These pins are not used in this modules.

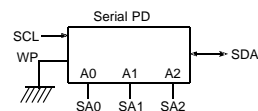
Functional Block Diagram



BA0 - BA1 → SDRAMs U0 - U15
 A0 - A12 → SDRAMs U0 - U15
 CEK0 → SDRAMs U0 - U7
 CEK1 → SDRAMs U8 - U15
 RAS# → SDRAMs U0 - U15
 CAS# → SDRAMs U0 - U15
 WE# → SDRAMs U0 - U15



| Clock Wiring | |
|--------------|----------|
| Clock Input | SDRAMs |
| CK0/CK0# | 8 SDRAMs |
| CK1/CK1# | 8 SDRAMs |





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Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -0.5 ~ 3.6 | V |
| Voltage on V _{DD} & V _{DDQ} supply relative to Vss | V _{DD} , V _{DDQ} | -1.0 ~ 3.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Operating temperature | T _A | 0 ~ 70 | °C |
| Power Dissipation | P _d | 16 | W |
| Short circuit output current | I _{OS} | 50 | mA |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating condition. Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

T_A = 0°C to 70°C

| Parameter | Symbol | Min | Max | Unit | Note | |
|--|----------------------|-------------------------|-------------------------|------|------|--|
| Supply voltage DDR333 (nominal V _{DD} 2.5V) | V _{DD} | 2.3 | 2.7 | V | | |
| IO Supply voltage DDR333 (nominal V _{DD} 2.5V) | V _{DDQ} | 2.3 | 2.7 | V | | |
| IO Reference voltage | V _{REF} | 0.49 * V _{DDQ} | 0.51 * V _{DDQ} | V | 1 | |
| IO Termination voltage | V _{TT} | V _{REF} -0.04 | V _{REF} +0.04 | V | 2 | |
| Input logic high voltage | V _{IH} (DC) | V _{REF} +0.15 | V _{DDQ} +0.30 | V | | |
| Input logic low voltage | V _{IL} (DC) | -0.3 | V _{REF} -0.15 | V | | |
| Input voltage level, CK and CK# | V _{IN} (DC) | -0.3 | V _{DDQ} +0.30 | V | | |
| Input differential voltage, CK and CK# | V _{ID} (DC) | 0.3 | V _{DDQ} +0.60 | V | 3 | |
| Input crossing point voltage, CK and CK# | V _{IX} (DC) | 0.3 | V _{DDQ} +0.60 | V | | |
| Input leakage current | Addr, CAS#,RAS#,WE# | I _I | -32 | 32 | µA | |
| | CS#, CKE | | -16 | 16 | µA | |
| | CK, CK# | | -16 | 16 | µA | |
| | DM | | -4 | 4 | µA | |
| Output leakage current | I _{OZ} | -10 | 10 | µA | | |
| Output high current(normal strength) V _{OUT} = v + 0.84V | I _{OH} | -16.8 | - | mA | | |
| Output high current(normal strength) V _{OUT} = V _{TT} - 0.84V | I _{OL} | 16.8 | - | mA | | |
| Output high current(half strength) V _{OUT} = V _{TT} + 0.45V | I _{OH} | -9 | - | mA | | |
| Output high current(half strength) V _{OUT} = V _{TT} - 0.45V | I _{OL} | 9 | - | mA | | |

Notes:

- V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed +/- 2% of the DC value.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level of CK#.



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AC Operating Conditions

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------------------|---------------------------|---------------------------|------|-------|
| Input High (Logic1) Voltage | V _{IH} (AC) | V _{REF} +0.31 | | V | 1 |
| Input Low (Logic0) Voltage | V _{IL} (AC) | | V _{REF} -0.31 | V | 1 |
| Input Differential Voltage, CK and CK# Inputs | V _{ID} (AC) | 0.7 | V _{DDQ} +0.6 | V | |
| Input Crossing Point Voltage, CK and CK# Inputs | V _{IX} (AC) | 0.5*V _{DDQ} -0.2 | 0.5*V _{DDQ} +0.2 | V | |

Notes: 1. V_{IH} overshoot: V_{IH} = V_{DDQ} + 1.5V for a pulse width <= 3ns and the pulse can not be greater than 1/3 of the cycle rate.
V_{IL} undershoot: V_{IL} = - 1.5V for a pulse width <= 3ns and the pulse can not be greater than 1/3 of the cycle rate.

Input/Output Capacitance

TA=25°C, f=100MHz

| Parameter | Symbol | Min | Max | Unit |
|--|------------------|-----|-----|------|
| Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#) | C _{IN1} | 28 | 44 | pF |
| Input capacitance (CKE0, CKE1) | C _{IN2} | 16 | 24 | pF |
| Input capacitance (CS0#, CS1#) | C _{IN3} | 16 | 24 | pF |
| Input capacitance (CK0, CK0#, CK1, CK1#) | C _{IN4} | 16 | 24 | pF |
| Input/Output capacitance (DQ, DQS, DM) | C _{IO} | 11 | 13 | pF |



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IDD Specification

| Condition | Symbol | -B3 | Unit |
|--|---------|------|------|
| OPERATING CURRENT: One device bank active; Active-Precharge; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles | IDD0* | 880 | mA |
| OPERATING CURRENT: One device bank; Active-Read-Precharge; BL=4; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; $I_{OUT}=0mA$; Address and control inputs change once per clock cycle | IDD1* | 1120 | mA |
| PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks are idle; Power-down mode; $t_{CK}=t_{CK(MIN)}$; CKE=LOW | IDD2P** | 80 | mA |
| IDLE STANDBY CURRENT: CS#=HIGH; All device banks are idle; $t_{CK}=t_{CK(MIN)}$; CKE=HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}=V_{REF}$ for DQ,DQS and DM | IDD2F** | 480 | mA |
| ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK}=t_{CK(MIN)}$; CKE=LOW | IDD3P** | 480 | mA |
| ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; One device bank active; $t_{RC}=t_{RAS(MAX)}$; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle | IDD3N** | 720 | mA |
| OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}=t_{CK(MIN)}$; $I_{OUT}=0mA$ | IDD4R* | 1160 | mA |
| OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change twice per clock cycle | IDD4W* | 1240 | mA |
| AUTO REFRESH CURRENT: $T_{RC}=T_{RFC(MIN)}$ | IDD5** | 3280 | mA |
| SELF-REFRESH CURRENT: CKE < 0.2V | IDD6** | 80 | mA |
| OPERATING CURRENT: Four device bank interleaving Reads Burst=4 with auto precharge; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands | IDD7* | 2920 | mA |
| <p>Note: IDD specification is based on Samsung F-die components. *: Value calculated as one module rank in this operation condition, and other module rank in IDD2P (CKE LOW) mode. **: Value calculated as all module ranks in this operation condition.</p> | | | |



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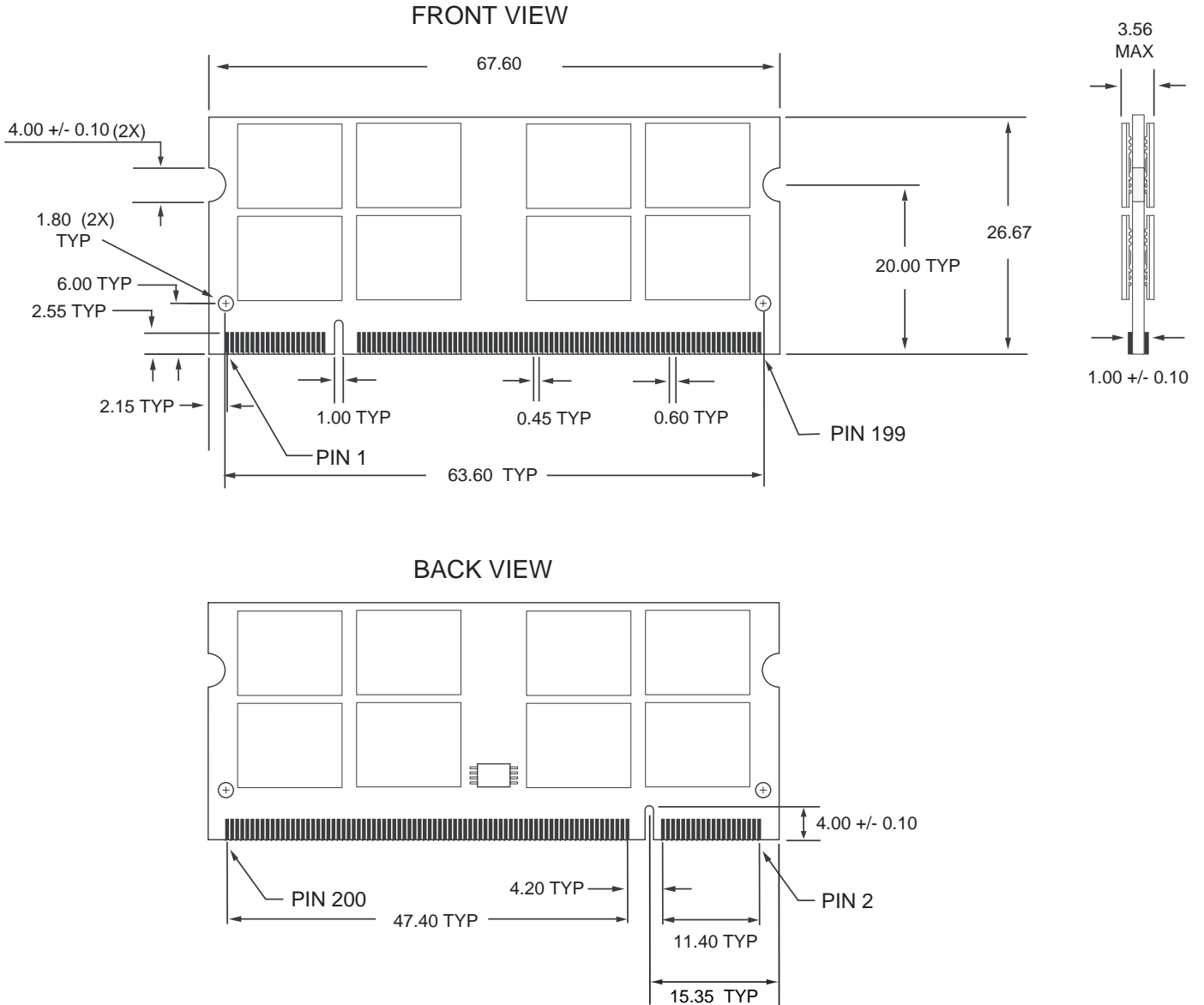
REV: 1.0

AC Timing Parameters & Specifications

| Parameter | Symbol | -B3 | | Unit |
|--|--------|-------------------------|------|------|
| | | MIN | MAX | |
| Row Cycle Time | tRC | 60 | | ns |
| Refresh row cycle time | tRFC | 72 | | ns |
| Row active | tRAS | 42 | 70K | ns |
| RAS# to CAS# delay | tRCD | 18 | | ns |
| Row precharge time | tRP | 18 | | ns |
| Row active to row active delay | tRRD | 12 | | ns |
| Write recovery time | tWR | 15 | | ns |
| Last data in to READ command | tWTR | 1 | | tCK |
| Clock cycle time | CL=2 | - | - | ns |
| | CL=2.5 | 6 | 12 | ns |
| | CL=3 | - | - | ns |
| Clock high level width | tCH | 0.45 | 0.55 | tCK |
| Clock low level width | tCL | 0.45 | 0.55 | tCK |
| DQS-out access time from CK/CK# | tDQSK | -0.6 | +0.6 | ns |
| Output data access time from CK/CK# | tAC | -0.7 | +0.7 | ns |
| Data strobe edge to output data edge | tDQSQ | - | 0.4 | ns |
| Read preamble | tRPRE | 0.9 | 1.1 | tCK |
| Read postamble | tRPST | 0.4 | 0.6 | tCK |
| CK to valid DQS-in | tDQSS | 0.75 | 1.25 | tCK |
| DQS-in setup time | tWPRES | 0 | | ns |
| DQS-in hold time | tWPRE | 0.25 | | tCK |
| DQS falling edge to CK rising-setup time | tDSS | 0.2 | | tCK |
| DQS falling edge to CK rising-hold time | tDSH | 0.2 | | tCK |
| DQS-in high level width | tDQSH | 0.35 | | tCK |
| DQS-in low level width | TDQSL | 0.35 | | tCK |
| Address and control input setup time (fast) | tISf | 0.75 | | ns |
| Address and control input hold time (fast) | tIHf | 0.75 | | ns |
| Address and control input setup time (slow) | tISs | 0.8 | | ns |
| Address and control input hold time (slow) | tIHs | 0.8 | | ns |
| Data-out high impedance time from CK/CK# | tHZ | -0.7 | +0.7 | ns |
| Data-out low impedance time from CK/CK# | tLZ | -0.7 | +0.7 | ns |
| Mode register set cycle | tMRD | 12 | | ns |
| DQ & DM setup time to DQS | tDS | 0.45 | | ns |
| DQ & DM hold time to DQS | tDH | 0.45 | | ns |
| Control & address input pulse width | tIPW | 2.2 | | ns |
| DQ & DM input pulse width | tDIPW | 1.75 | | ns |
| Exit self refresh to non-Read command | tXSNR | 75 | | ns |
| Exit self refresh to Read command | tXSRD | 200 | | tCK |
| Refresh interval time | tREFI | | 7.8 | us |
| Output DQS valid window | tQH | tHP -tQHS | - | ns |
| Clock half period | tHP | tCLmin or tCHmin | - | ns |
| Data hold skew factor | tQHS | | 0.5 | ns |
| DQS write postamble | tWPST | 0.4 | 0.6 | tCK |
| Active Read with auto precharge command | tRAP | 18 | | |
| Auto precharge Write recovery + Precharge time | tDAL | tWR/tCK + tRP/tCK | | tCK |

| | | |
|---------------------------------|-----------------|----------|
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Package Dimensions



NOTE:
 All dimension are in millimeters with tolerance +/- 0.15mm unless otherwise specified.



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Revision History:

| Date | Rev. | Page | Changes |
|----------|------|------|--------------|
| 04/02/09 | 1.0 | All | Spec release |
| | | | |
| | | | |