

Product Specifications		
PART NO.:	VL393T5263F-F7Y/E7Y/E6Y	REV: 1.0

## General Information

### 4GB 512Mx72 DDR2 SDRAM ULP REGISTERED ECC DIMM 240-PIN

## Description

The VL393T5263F is a 512Mx72 DDR2 SDRAM high density DIMM. This memory module consists of eighteen CMOS 256Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, two 25-bit registered buffers in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin MLF package. This module is a 240-pin dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

## Features

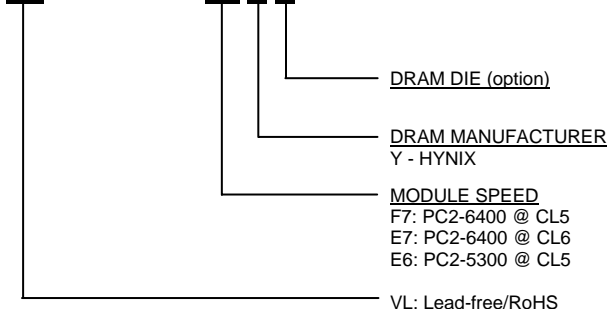
- 240-pin, dual in-line memory module (DIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rates: PC2-6400, PC2-5300
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL\_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 5, 6 (DDR2-800), 5 (DDR2-667)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD)
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 17.78mm (0.700”), double sided components

## Pin Description

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK0, CK0#	Clock Input
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
CB0~CB7	Check Bits
DM0~DM8/ DQS9~DQS17	Data Masks/ Data Strobes (Read)
DQS9# ~ DQS17#	Data Strobes Complement (Read)
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

## Order Information:

**VL393T5263F-F7 Y X**





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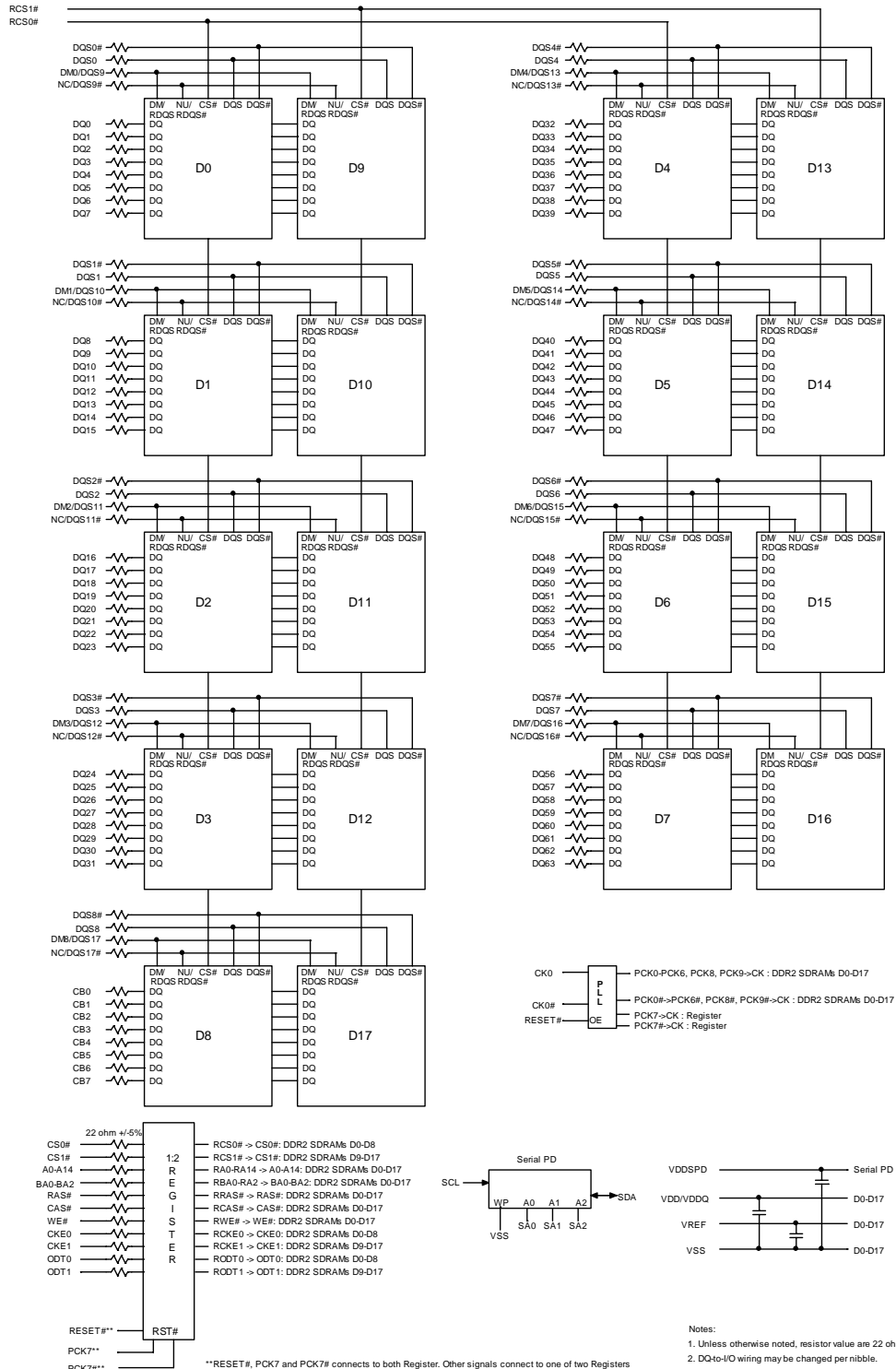
VL393T5263F-F7Y/E7Y/E6Y

REV: 1.0

## Pin Configuration

240-PIN DDR2 DIMM FRONT								240-PIN DDR2 DIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5/DQS14
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC/DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0/DQS9	155	DM3/DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC/DQS9#	156	NC/DQS12#	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	NC
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	NC
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	VSS
13	DQ9	43	CB1	73	WE#	103	VSS	133	VSS	163	VSS	193	CS0#	223	DM6/DQS15
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1/DQS10	164	DM8/DQS17	194	VDDQ	224	NC/DQS15#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	NC/DQS10#	165	NC/DQS17#	195	ODT0	225	VSS
16	DQS1	46	DQS8	76	CS1#	106	VSS	136	VSS	166	VSS	196	A13	226	DQ54
17	VSS	47	VSS	77	ODT1	107	DQ50	137	NC	167	CB6	197	VDD	227	DQ55
18	RESET#	48	CB2	78	VDDQ	108	DQ51	138	NC	168	CB7	198	VSS	228	VSS
19	NC	49	CB3	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4/DQS13	232	DM7/DQS16
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC/DQS13#	233	NC/DQS16#
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	A14	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2/DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC/DQS11#	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

## Function Block Diagram



<b>Product Specifications</b>		
PART NO.:	VL393T5263F-F7Y/E7Y/E6Y	REV: 1.0

<b>Absolute Maximum Ratings</b>					
Symbol	Parameter	MIN	MAX	Unit	
VDD	Voltage on VDD pin relative to VSS	-1.0	2.3	V	
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5	2.3	V	
VDDL	Voltage on VDDL pin relative to VSS	-0.5	2.3	V	
VIN, VOUT	Voltage on any pin relative to VSS	-0.5	2.3	V	
TSTG	Storage temperature	-55	100	°C	
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-10	10	uA
		CS#, CKE, ODT	-10	10	uA
		CK, CK#	-250	250	uA
		DM	-4	4	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-36	36	uA

<b>DC Operating Conditions</b>						
Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Note:

- VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
- VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
- VDDQ tracks with VDD; VDDL tracks with VDD.

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Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 95	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 – 85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TOPER <= 95°C.				

Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.200	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	9	11	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	9	11	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	9	11	pF

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## IDD Specification

Condition	Symbol	-F7	-E7	-E6	Unit
<b>Operating one bank active-pre-charge;</b> $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS\ MIN(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1463	1463	1418	mA
<b>Operating one bank active-read-pre-charge;</b> IOU = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS\ MIN(IDD)}$ ; $t_{RCD} = t_{RCD(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1	1553	1553	1508	mA
<b>Pre-charge power-down current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	716	716	716	mA
<b>Pre-charge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	1400	1400	1310	mA
<b>Pre-charge standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING.	IDD2N	1490	1490	1400	mA
<b>Active power-down current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P	Fast PDN Exit MRS(12) = 0	1130	1130	1130
		Slow PDN Exit MRS(12) = 1	824	824	824
<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	1940	1940	1760	mA
<b>Operating burst write current;</b> All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W	2768	2768	2408	mA
<b>Operating burst read current;</b> All banks open; Continuous burst reads; IOU = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R	2588	2588	2273	mA
<b>Burst refresh current;</b> $t_{CK} = t_{CK(IDD)}$ ; Refresh command at every $t_{RFC(IDD)}$ interval; CE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	4640	4640	4460	mA
<b>Self refresh current;</b> CK and CK# at 0V; CE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6	270	270	270
<b>Operating bank interleave read current;</b> All bank interleaving reads; IOU = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$ ; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RRD} = t_{RRD(IDD)}$ ; $t_{RCD} = 1 * t_{CK(IDD)}$ ; CE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7	3353	3353	3128	mA

Notes: IDD specification is based on Hynix A-die components.

\*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P ( CE LOW) mode.

\*\*: Value calculated reflects all module ranks in this operating condition.

# Product Specifications

**PART NO.:**
**VL393T5263F-F7Y/E7Y/E6Y**
**REV: 1.0**

## AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-800 (-F7/-E7)		DDR2-667 (-E6)		Unit	
		Min	Max	Min	Max		
<b>Clock Timing</b>							
Clock Cycle Time	CL6	$t_{CK(6)}$	2,500	8,000	-	-	ps
	CL5	$t_{CK(5)}$	3,000	8,000	3,000	8,000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	0.48	0.52	$t_{CK}$
CK high-level width		$t_{CL(avg)}$	0.48	0.52	0.48	0.52	$t_{CK}$
Half clock period		$t_{HP}$	MIN ( $t_{CH}$ , $t_{CL}$ )	-	MIN ( $t_{CH}$ , $t_{CL}$ )	-	ps
Clock jitter		$t_{JIT}$	-100	100	-125	125	ps
<b>Data Timing</b>							
DQ output access time from CK/CK#		$t_{AC}$	-400	400	-450	+450	ps
Data-out high impedance window from CK/CK#		$t_{HZ}$	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		$t_{LZ}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		$t_{DS}$	50	-	100	-	ps
DQ and DM input hold time relative to DQS		$t_{DH}$	125	-	175	-	ps
DQ and DM input pulse width ( for each input)		$t_{DIPW}$	0.35	-	0.35	-	$t_{CK}$
Data hold skew factor		$t_{QHS}$	-	300	-	340	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		$t_{QH}$	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	ps
<b>Data Strobe Timing</b>							
DQS input high pulse width		$t_{DQSH}$	0.35	-	0.35	-	$t_{CK}$
DQS input low pulse width		$t_{DQSL}$	0.35	-	0.35	-	$t_{CK}$
DQS output access time from CK/CK#		$t_{DQSCK}$	-350	+350	-400	+400	ps
DQS failing edge to CK rising-setup time		$t_{DSS}$	0.2	-	0.2	-	$t_{CK}$
DQS failing edge from CK rising-hold time		$t_{DSH}$	0.2	-	0.2	-	$t_{CK}$
DQS-DQ skew, DQS to last DQ valid, per group, per access		$t_{DQSQ}$	-	200	-	240	ps
DQS read preamble		$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$
DQS read preamble		$t_{RPST}$	0.4	0.6	0.4	0.6	$t_{CK}$
DQS read preamble		$t_{WPRE}$	0.35	-	0.35	-	$t_{CK}$
DQS read preamble		$t_{WPST}$	0.4	0.6	0.4	0.6	$t_{CK}$
Write command to first DQS latching transition		$t_{DQSS}$	WL-0.25	WL+0.25	WL-0.25	WL+0.25	$t_{CK}$



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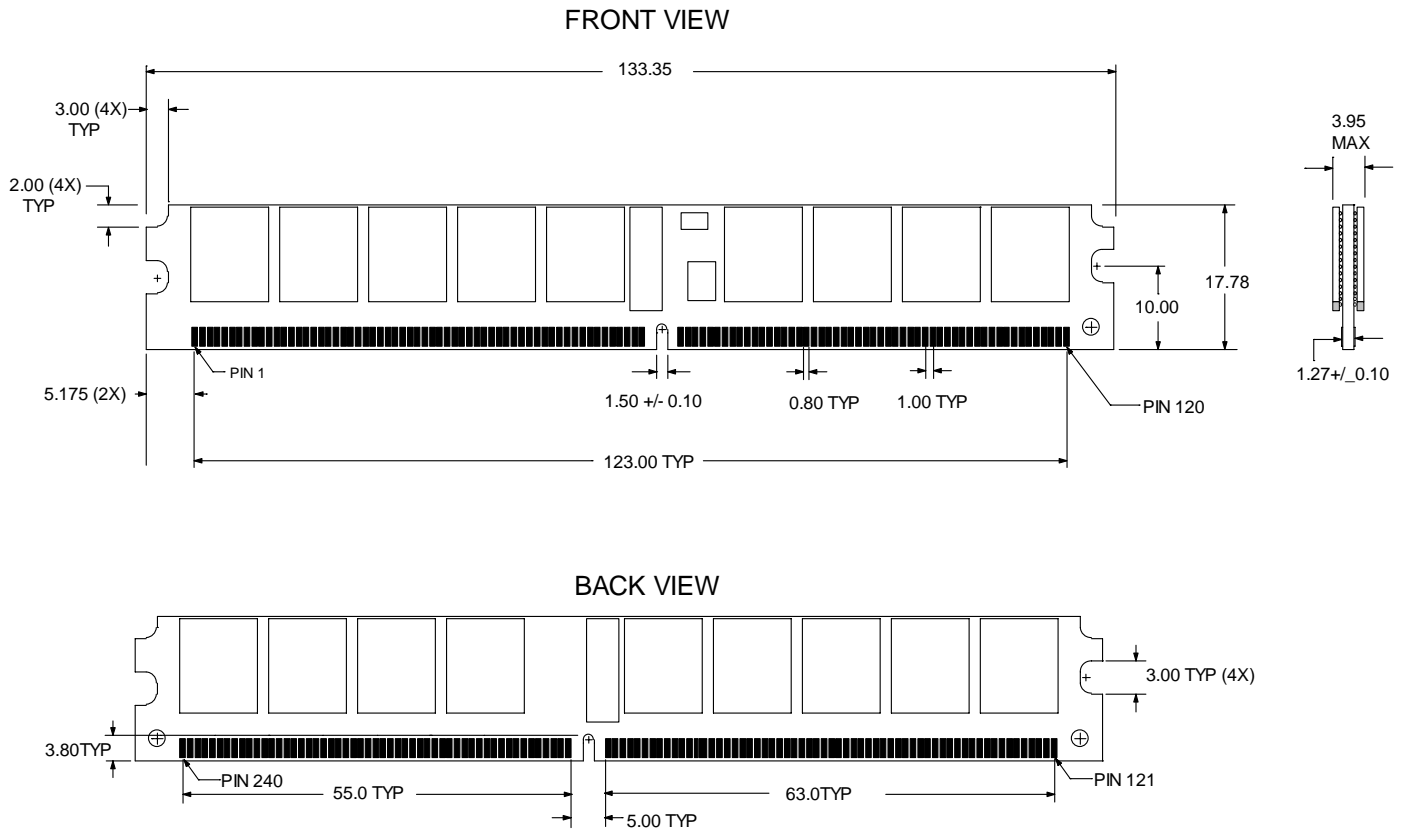
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## AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-800 (-F7/-E7)		DDR2-667 (-E6)		Unit
		Min	Max	Min	Max	
<b>Command and Address Timing</b>						
Address and control input pulse width for each input	$t_{IPW}$	0.6	-	0.6	-	$t_{CK}$
Address and control input setup time	$t_{IS}$	175	-	200	-	ps
Address and control input hold time	$t_{IH}$	250	-	275	-	ps
CAS# to CAS# command delay	$t_{CCD}$	2	-	2	-	ps
ACTIVE to ACTIVE (same bank) command	$t_{RC}$	57.5/60	-	60	-	ns
ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	$t_{RCD}$	12.5/15	-	15	-	ns
Four Bank Activate period	$t_{FAW}$	35	-	37.5	-	ns
ACTIVE to PRECHARGE command	$t_{RAS}$	45	70,000	45	70,000	ns
Internal READ to precharge Command delay	$t_{RTP}$	7.5	-	7.5	-	ns
Write recovery time	$t_{WR}$	15	-	15	-	ns
Auto precharge write recovery + precharge time	$t_{DAL}$	$t_{WR}+t_{nRP}$	-	$t_{WR}+t_{nRP}$	-	nCK
Internal WRITE to READ Command delay	$t_{WTR}$	7.5	-	7.5	-	ns
PRECHARGE command period	$t_{RP}$	15	-	15	-	ns
LOAD MODE command cycle time	$t_{MRD}$	2	-	2	-	$t_{CK}$
CKE low to CK, CK# uncertainty	$t_{DELAY}$	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	ns
<b>Self Refresh</b>						
Refresh to Active or Refresh to Refresh command interval	$t_{RFC}$	195	-	195	-	ns
Average periodic Refresh interval	$t_{REFI}$	-	7.8	-	7.8	us
Exit Self Refresh to non-READ command	$t_{XSNR}$	$t_{RFC(MIN)}+10$	-	$t_{RFC(MIN)}+10$	-	ns
Exit Self Refresh to READ	$t_{XSRD}$	200	-	200	-	$t_{CK}$
<b>ODT</b>						
ODT turn-on delay	$t_{AOND}$	2	2	2	2	$t_{CK}$
ODT turn-on	$t_{AON}$	$t_{AC(MIN)}$	$t_{AC(MAX)}+700$	$t_{AC(MIN)}$	$t_{AC(MAX)}+700$	ps
ODT turn-off delay	$t_{AOFD}$	2.5	2.5	2.5	2.5	$t_{CK}$
ODT turn-off	$t_{AOF}$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	ps
ODT turn-on(power-down mode)	$t_{AONPD}$	$t_{AC(MIN)}+2,000$	$2t_{CK}+t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2,000$	$2t_{CK}+t_{AC(MAX)}+1,000$	ps
ODT turn-off (power-down mode)	$t_{AOFDP}$	$t_{AC(MIN)}+2,000$	$2.5t_{CK}+t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2,000$	$2.5t_{CK}+t_{AC(MAX)}+1,000$	ps
ODT to power-down entry latency	$t_{ANPD}$	3	-	3	-	$t_{CK}$
ODT power-down exit latency	$t_{AXPD}$	8	-	8	-	$t_{CK}$
OCD drive mode output delay	$t_{OIT}$	0	1,200	0	1,200	ps
<b>Power Down</b>						
Exit active power-down to READ command, MR[bit12=0]	$t_{XARD}$	2	-	2	-	$t_{CK}$
Exit active power-down to READ command, MR[bit12=1]	$t_{XARDS}$	8-AL	-	7-AL	-	$t_{CK}$
Exit precharge power-down to any non-READ command	$t_{XP}$	2	-	2	-	$t_{CK}$
CKE minimum high/low time	$t_{CKE}$	3	-	3	-	$t_{CK}$

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## Package Dimensions



- Note: 1. All dimension are in millimeters with tolerance +/- 0.15mm unless otherwise specified.  
 2. The dimensional diagram is for reference only.



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**Revision History:**

Date	Rev.	Page	Changes
12/19/09	1.0	All	Spec release