



Product Specifications

PART NO:

VL368L2923E-B3S/A2S/B0S

REV:

1.3

General Information

1GB 128MX64 DDR SDRAM NON-ECC UNBUFFERED DIMM 184-PIN

Description: The VL368L2923E is a 128M X 64 Double Data Rate SDRAM high density unbuffered DIMM. This memory module consists of 16 CMOS 64Mx8 bit with 4 banks DDR Synchronous DRAMs in TSOP-II 400 mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 184-pin Dual In-line Memory Module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR SDRAM.

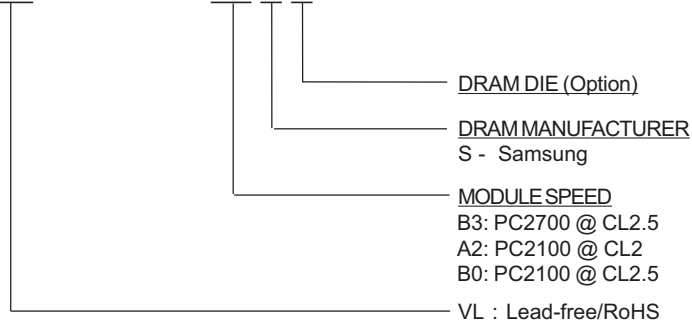
Features:

- . Power supply : Vdd: 2.5V +/- 0.2V, Vddq: 2.5V +/- 0.2V
- . Two data transfers per clock cycle
- . Bidirectional data strobe (DQS)
- . Differential clock inputs (CK and CK#)
- . DLL aligns DQ and DQS transition with CK transition
- . Programmable Read latency 2, 2.5 (clock)
- . Programmable Burst ; length (2, 4, 8)
- . Programmable Burst (sequential & Interleave)
- . Auto & Self refresh, (8K/64ms refresh)
- . Serial presence detect with EEPROM
- . PCB: **Height 1125 (mil)**, double sided component
- . Gold edge contacts
- . Lead-Free/RoHS compliant

Pin Name	Function
A0-A12	Address inputs
BA0,BA1	Bank Selct Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0,CK0# ~ CK2,CK2#	Clock Input
CKE0,CKE1	Clock Enable Input
CS0#,CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DM0-DM7	Data Mask
VDD	Power Supply
VDDQ	Power Supply for DQS
VSS	Ground
VREF	Power Supply for Reference
VDDSPD	SPD Power Supply (2.3V-3.6V)
SDA	Serial Data Input/Output
SCL	SPD Clock Input
SA0-SA2	SPD Address
NC	No Connect

Order Information

VL368L2923E-B3 S X





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Pin Configuration															
184-PIN DDR DIMM FRONT								184-PIN DDR DIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	24	DQ17	47	DQS8*	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DM8*	163	NC
3	VSS	26	VSS	49	CB2*	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DM2	142	CB6*	165	DQ52
5	DQS0	28	DQ18	51	CB3*	74	VSS	97	DM0	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	CK2#	98	DQ6	121	DQ22	144	CB7*	167	A13*
7	VDD	30	VDDQ	53	DQ32	76	CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DM6
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	NC	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DM4	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	NC	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	VSS
16	CK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS#	177	DM7
17	CK1#	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	CKE1	134	CB4*	157	CS0#	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5*	158	CS1#	181	SA0
21	CKE0	44	CB0*	67	DQS5	90	NC	113	NC	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	CB1*	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	CK0#	161	DQ46	184	VDD-SPD

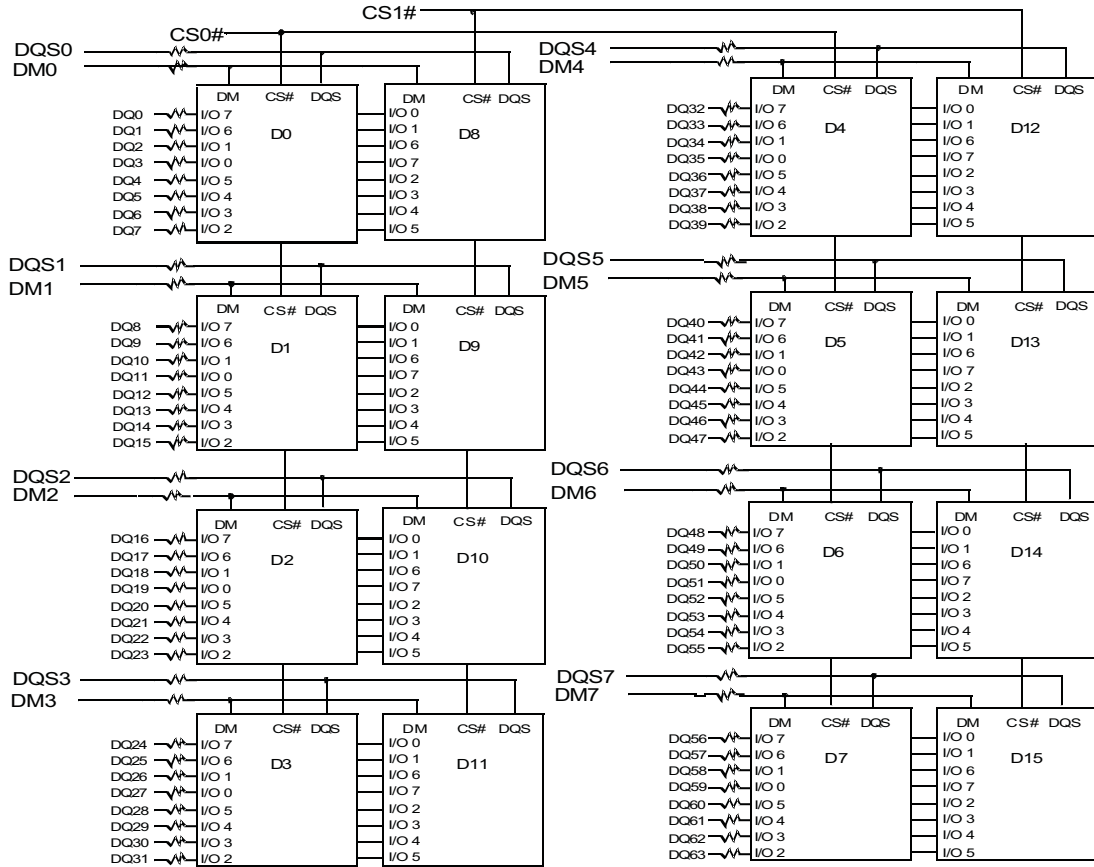
Note: *: These pins are not used on this module.

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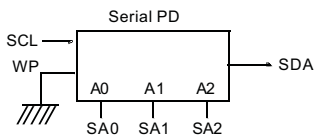
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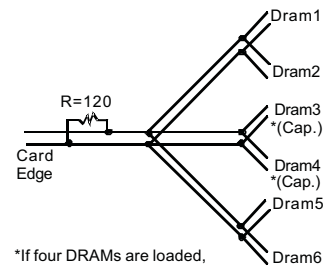
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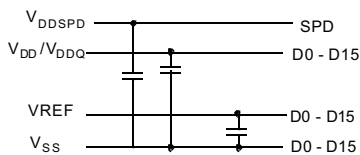
*Clock Net Wiring



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0#	4 SDRAMs
CK1/CK1#	6 SDRAMs
CK2/CK2#	6 SDRAMs


 *If four DRAMs are loaded,
 Cap will replace DRAM3,4

- BA0 - BA1 → BA0-BA1: SDRAMs D0 - D15
- A0 - A12 → A0-A12: SDRAMs D0 - D15
- RAS# → RAS#: SDRAMs D0 - D15
- CAS# → CAS#: SDRAMs D0 - D15
- CKE1 → CKE: SDRAMs D8 - D15
- CKE0 → CKE: SDRAMs D0 - D7
- WE# → WE# SDRAMs D0 - D15


Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM resistors: 22 Ohms.



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on V _{DD} & V _{DDQ} supply relative to V _{SS}	V _{DD} , V _{DDQ}	-0.1 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Operating temperature	T _A	0 ~ 70	°C
Power Dissipation	P _D	16	W
Short circuit output current	I _{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating condition. Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

T_A = 0°C to 70°C

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V _{DD} 2.5V)		V _{DD}	2.3	2.7	V	
I/O Supply voltage DDR266/DDR333 (nominal V _{DD} 2.5V)		V _{DDQ}	2.3	2.7	V	
I/O Reference voltage		V _{REF}	0.49 * V _{DDQ}	0.51 * V _{DDQ}	V	1
I/O Termination voltage		V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage		V _{IH} (DC)	V _{REF} +0.15	V _{DDQ} +0.30	V	
Input logic low voltage		V _{IL} (DC)	-0.3	V _{REF} -0.15	V	
Input voltage level, CK and CK#		V _{IN} (DC)	-0.3	V _{DDQ} +0.30	V	
Input differential voltage, CK and CK#		V _{ID} (DC)	0.36	V _{DDQ} +0.60	V	3
Input crossing point voltage, CK and CK#		V _{IX} (DC)	0.3	V _{DDQ} +0.60	V	
Input leakage current	Addr, CAS#,RAS#,WE#	I _I	-32	32	uA	
	CS#, CKE		-16	16	uA	
	CK, CK#		-12	12	uA	
	DM		-4	4	uA	
Output leakage current		I _{OZ}	-10	10	uA	
Output high current(normal strength) V _{OUT} = v + 0.84V		I _{OH}	-16.8	-	mA	
Output high current(normal strength) V _{OUT} = V _{TT} - 0.84V		I _{OL}	16.8	-	mA	
Output high current(half strength) V _{OUT} = V _{TT} + 0.45V		I _{OH}	-9	-	mA	
Output high current(half strength) V _{OUT} = V _{TT} - 0.45V		I _{OL}	9	-	mA	

Notes:

- V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed +/- 2% of the DC value.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level of CK#.



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AC Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
Input High (Logic1) Voltage	VIH(AC)	VREF+0.31		V	1
Input Low (Logic0) Voltage	VIL(AC)		VREF-0.31	V	1
Input Differential Voltage, CK and CK# inputs	VID(AC)	0.7	VDDQ+0.6	V	
Input Crossing Point Voltage, CK and CK# input	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	

Notes: 1. VIH overshoot: $V_{IH} = V_{DDQ} + 1.5V$ for a pulse width $\leq 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.
 VIL undershoot: $V_{IL} = -1.5V$ for a pulse width $\leq 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.

Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1,RAS#,CAS#,WE#)	CIN1	36	52	pF
Input capacitance (CKE0,CKE1)	CIN2	20	28	pF
Input capacitance (CS0#,CS1#)	CIN3	20	28	pF
Input capacitance (CK0,CK0# ~ CK2,CK2#)	CIN4	16	22	pF
Input capacitance (DQS0 ~ DQS7), (DM0 ~ DM7)	CIN5	12	14	pF
Input capacitance (DQ0 ~ DQ63)	COUT1	12	14	pF



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IDD Specification

Condition	Symbol	-B3	-A2	-B0	Unit
OPERATING CURRENT: One device bank active; Active-Precharge; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	IDD0*	880	800	800	mA
OPERATING CURRENT: One device bank; Active-Read-Precharge; BL=4; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; $I_{OUT}=0mA$; Address and control inputs change once per clock cycle	IDD1*	1120	1040	1040	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks are idle; Power-down mode; $t_{CK}=t_{CK(MIN)}$; CKE=LOW	IDD2P**	80	80	80	mA
IDLE STANDBY CURRENT: CS#=HIGH; All device banks are idle; $t_{CK}=t_{CK(MIN)}$; CKE=HIGH; Address and other control inputs changing once per clock cycle. $V_{IN}=V_{REF}$ for DQ,DQS and DM	IDD2F**	480	480	480	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; $t_{CK}=t_{CK(MIN)}$; CKE=LOW	IDD3P**	480	480	480	mA
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; One device bank active; $t_{RC}=t_{RAS(MAX)}$; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N**	720	720	720	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}=t_{CK(MIN)}$; $I_{OUT}=0mA$	IDD4R*	1160	1040	1040	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK}=t_{CK(MIN)}$; DQ,DM and DQS inputs change twice per clock cycle	IDD4W*	1240	1080	1080	mA
AUTO REFRESH CURRENT: $T_{RC}=T_{RFC(MIN)}$	IDD5**	3280	3120	3120	mA
SELF-REFRESH CURRENT: CKE < 0.2V	IDD6**	80	80	80	mA
OPERATING CURRENT: Four device bank interleaving Reads Burst=4 with auto precharge; $t_{RC}=t_{RC(MIN)}$; $t_{CK}=t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands	IDD7*	2920	2640	2640	mA
<p>Note: IDD specification is based on Samsung components. Other DRAM Manufacturers specification may be different. *: Value calculated as one module rank in this operation condition, and other module rank in IDD2P (CKE LOW) mode. **: Value calculated as all module ranks in this operation condition.</p>					



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AC Timing Parameters & Specifications

Parameter	Symbol	-B3		-A2		-B0		Unit
		Min	Max	Min	Max	Min	Max	
Row Cycle Time	t _{RC}	60		65		65		tCK
Refresh row cycle time	t _{RFC}	72		75		75		ps
Row active	t _{RAS}	42	70K	45	120K	45	120K	ps
RAS# to CAS# delay	t _{RCd}	18		20		20		tCK
Row precharge time	t _{RP}	18		20		20		ns
Row active to row active delay	t _{RRD}	12		15		15		ns
Write recovery time	t _{WR}	15		15		15		ns
Last data in to READ command	t _{WTR}	1		1		1		ns
Clock cycle time	CL=2	7.5	12	7.5	12	7.5	12	ns
	CL=2.5	6	12	7.5	12	7.5	12	ns
	CL=3	-	-	-	-	-	-	ns
Clock high level width	t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock low level width	t _{CL}	0.55	0.55	0.55	0.55	0.55	0.55	tCK
DQS-out access time from CK/CK#	t _{DQsck}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns
Output data access time from CK/CK#	t _{Ac}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Data strobe edge to output data edge	t _{DQsQ}	-	0.45	-	0.5	-	0.5	ns
Read preamble	t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	tCK
CK to valid DQS-in	t _{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS-in setup time	t _{WPRES}	0		0		0		ns
DQS-in hold time	t _{WPRE}	0.25		0.25		0.25		tCK
DQS falling edge to CK rising-setup time	t _{DSS}	0.2		0.2		0.2		tCK
DQS falling edge to CK rising-hold time	t _{DSH}	0.2		0.2		0.2		tCK
DQS-in high level width	t _{DQSH}	0.35		0.35		0.35		tCK
DQS-in low level width	t _{DQSL}	0.35		0.35		0.35		tCK
Address and control input setup time (fast)	t _{IS}	0.75		0.9		0.9		ns
Address and control input hold time (fast)	t _{IH}	0.75		0.9		0.9		ns
Address and control input setup(slow)p	t _{IS}	0.7		0.7		0.7		ns
Address and control input hold time (slow)	t _{IH}	0.7		0.7		0.7		ns
Data-out high impedance time from CK/CK#	t _{HZ}	-0.7	+0.7		+0.75		+0.75	ns
Data-out low impedance time from CK/CK#	t _{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Mode register set cycle	t _{MRD}	10		10		10		ns
DQ & DM setup time to DQS	t _{DS}	0.4		0.4		0.4		ns
DQ & DM hold time to DQS	t _{DH}	0.4		0.4		0.4		ns
Control & address input pulse width	t _{IPW}	2.2		2.2		2.2		ns
DQ & DM input pulse width	t _{DIPW}	1.75		1.75		1.75		ns
Exit self refresh to non-Read command	t _{XSNR}	75		75		75		ns
Exit self refresh to Read command	t _{XSRD}	200		200		200		tCK
Refresh interval time	t _{REFI}		7.8		7.8		7.8	us
Output DQS valid window	t _{QH}	t _{HP} -t _{QHS}	-	t _{HP} -t _{QHS}	-	t _{HP} -t _{QHS}	-	ns
Clock half period	t _{HP}	t _{CLmin} or t _{CHmin}	-	t _{CLmin} or t _{CHmin}	-	t _{CLmin} or t _{CHmin}	-	ns
Data hold skew factor	t _{QHS}		0.55		0.75		0.75	ns
DQS write postamble	t _{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	ns
Active Read with auto precharge command	t _{RAP}	18		20		20		ns
Auto precharge Write recovery + Precharge time	t _{RAL}	t _{WR} /t _{CK} + t _{RP} /t _{CK}		t _{WR} /t _{CK} + t _{RP} /t _{CK}		t _{WR} /t _{CK} + t _{RP} /t _{CK}		tCK

