



# Product Specifications

PART NO:

**VL33B5663F-K9M-F8M-E7M**

REV: **1.1**

## General Information

### 2GB 256MX72 DDR3 SDRAM ULP ECC RDIMM 240 PIN

**Description** The VL33B5663F is a 256Mx72 DDR3 SDRAM high density RDIMM. This memory module consists of eighteen CMOS 128Mx8 bit with 8 banks DDR3 Synchronous DRAMs in BGA packages, a 28-bit registered buffer/PLL clock in BGA package, and a 2K EEPROM in an 8-pin MLF package. This module is a 240-pin dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

### Features

- . 240-pin, dual-in line memory module (RDIMM)
- . JEDEC pin-out
- . Fast data transfer rates: PC3-10600, PC3-8500, PC3-6400
- . VDD = VDDQ = 1.5V +/- 0.075V
- . VDDSPD = 3V to 3.6V
- . JEDEC standard 1.5V +/- 0.075V I/O (SSTL\_15 compatible)
- . Eight internal component banks for concurrent operation
- . 8-bit pre-fetch architecture
- . Bi-directional differential data-strobe
- . Programmable CAS# latency: 9 (DDR3-1333), 7 (DDR3-1066) 6 (DDR3-800)
- . Programmable burst length (8)
- . On-die termination (ODT)
- . Average refresh period 7.8 us
- . Serial presence detect (SPD) with thermal sensor
- . Thermal sensor range: -20°C to +125°C (+/- 1°C Accuracy)
- . Asynchronous Reset
- . Fly-by topology
- . Terminated command, address, and control bus
- . Gold edge PCB contacts
- . Lead-free, RoHS compliant
- . PCB: Height 17.78mm (0.700"), double sided components

Pin Name	Function
A0-A13	Address Inputs
A10/AP	Address Inputs/ Auto Precharge
A12/BC#	Address Input/ Burst Chop
BA0-BA2	Bank Address Inputs
DQ0-DQ63	Data Input/Output
DQS0-DQS8	Data Strobes
DQS0#-DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK0, CK0#, CK1, CK1#	Clock Input
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply 1.5V +/- 0.075V
VSS	Ground
SA0-SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
DM0-DM8/ DQS9-DQS17	Data Masks/ Data Strobes (Read)
DQS9#-DQS17#	Data Strobes Complement (Read)
CB0-CB7	Data Check Bits I/O
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply 3V to 3.6V
VTT	Termination Voltage
RESET#	Register and SDRAM Control
EVENT#	Reserved for Temp Sensing
NC	No Connect

## Order Information

**VL33B5663F-F8 M X**

DRAM DIE (Option)

DRAM MANUFACTURER  
M - MICRON

MODULE SPEED  
K9: PC3-10600 @ CL9  
F8: PC3-8500 @ CL7  
E7: PC3-6400 @ CL6

VL : Lead-free/RoHS



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## Pin Configuration

240-PIN DDR3 RDIMM FRONT								240-PIN DDR3 RDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3/ DQS12/ TDQS12	182	VDD	212	DM5/ DQS14/ TDQS14
3	DQ0	33	DQS3#	63	CK1	93	DQS5#	123	DQ5	153	NC/ DQS12#/ TDQS12#	183	VDD	213	NC/ DQS14#/ TDQS14#
4	DQ1	34	DQS3	64	CK1#	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0/ DQS9/ TDQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	NC/ DQS9#/ TDQS9#	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	EVENT# NC	217	VSS
8	VSS	38	VSS	68	PAR_IN/ NC	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DM8/ DQS17/ TDQS17	191	VDD	221	DM6/ DQS15/ TDQS15
12	DQ8	42	DQS8#	72	VDD	102	DQS6#	132	DQ13	162	NC/ DQS17#/ TDQS17#	192	RAS#	222	NC/ DQS15#/ TDQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	VSS	163	VSS	193	CS0#	223	VSS
14	VSS	44	VSS	74	CAS#	104	VSS	134	DM1/ DQS10/ TDQS10	164	CB6	194	VDD	224	DQ54
15	DQS1#	45	CB2	75	VDD	105	DQ50	135	NC/ DQS10#/ TDQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	CS1#	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC/ TEST	197	VDD	227	DQ60
18	DQ10	48	VTT/ NC	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	CS3#*	228	DQ61
19	DQ11	49	VTT/ NC	79	CS2#*	109	DQ57	139	VSS	169	CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7/ DQS16/ TDQS16
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	A15*	201	DQ37	231	NC/ DQS16#/ TDQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14*	202	VSS	232	VSS
23	VSS	53	ERR_OUT / NC	83	VSS	113	VSS	143	DM2/ DQS11/ TDQS11	173	VDD	203	DM4/ DQS13/ TDQS13	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	NC/ DQS11#/ TDQS11#	174	A12/BC#	204	NC/ DQS13#/ TDQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

\* These pins are not used in this module.



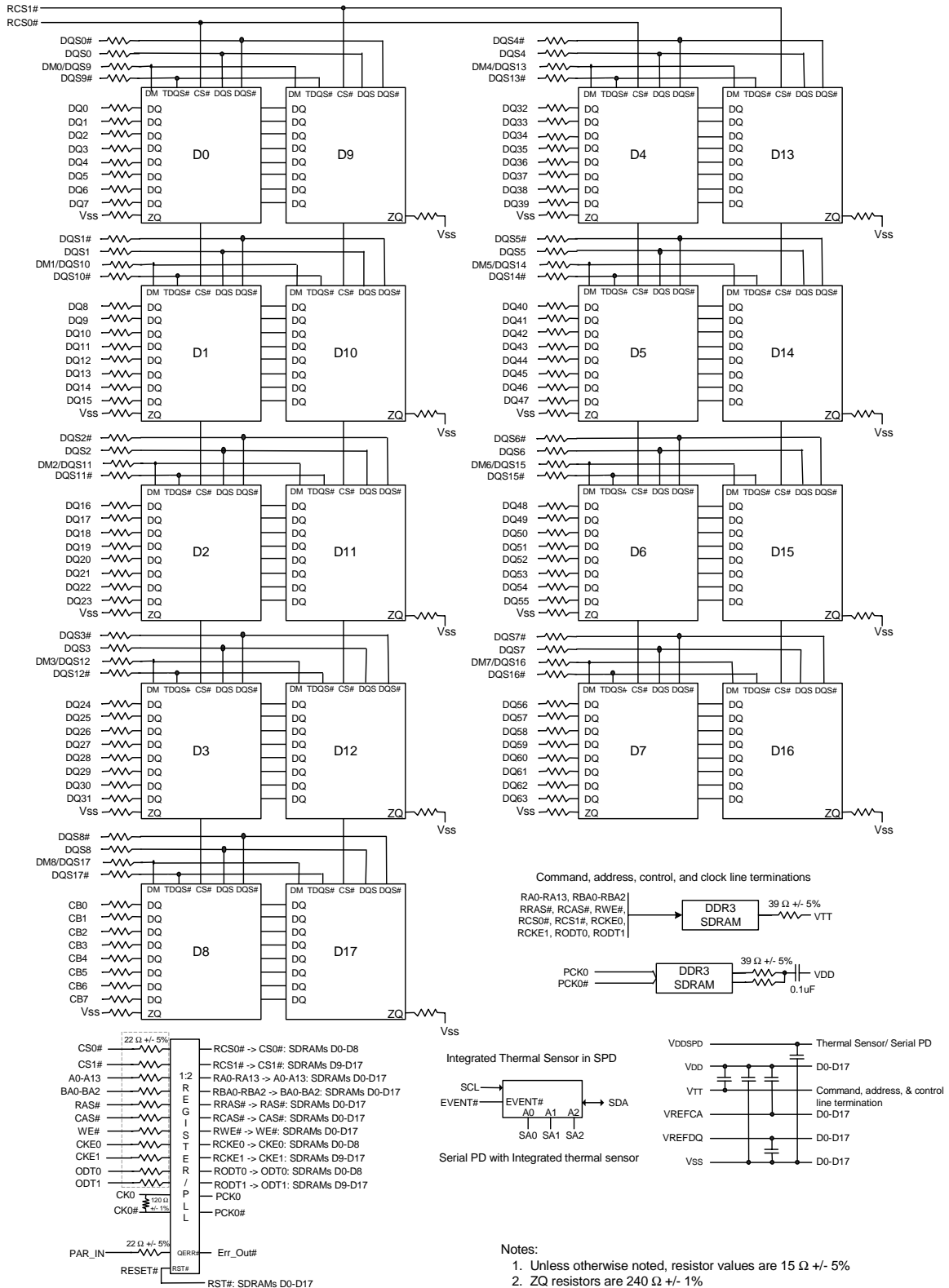
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## Functional Block Diagram





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## Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit	
V <sub>DD</sub>	Voltage on V <sub>DD</sub> pin relative to V <sub>SS</sub>	-0.4	1.975	V	
V <sub>DDQ</sub>	Voltage on V <sub>DDQ</sub> pin relative to V <sub>SS</sub>	-0.4	1.975	V	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.4	1.975	V	
T <sub>STG</sub>	Storage temperature	-55	150	°C	
I <sub>L</sub>	Input leakage current; Any input 0V < V <sub>IN</sub> < V <sub>DD</sub> ; VREF input 0V < V <sub>IN</sub> < 0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, CS#, CE, ODT, BA	-5	5	µA
		CK, CK#	-5	5	µA
		DM	-4	4	µA
I <sub>OZ</sub>	Output leakage current; 0V < V <sub>OUT</sub> < V <sub>DDQ</sub> ; DQs and ODT are disabled	-10	10	µA	
I <sub>VREF</sub>	VREF leakage current; VREF = Valid VREF level	-18	18	µA	

## DC Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V <sub>DD</sub>	1.425	1.5	1.575	V	1,2
Supply Voltage for Output	V <sub>DDQ</sub>	1.425	1.5	1.575	V	1,2
I/O Reference voltage (DQ)	VREFDQ (DC)	0.49 x V <sub>DD</sub>	0.5 x V <sub>DD</sub>	0.51 x V <sub>DD</sub>	V	3,4
I/O Reference voltage (CMD/ADD)	VREFCA (DC)	0.49 x V <sub>DD</sub>	0.5 x V <sub>DD</sub>	0.51 x V <sub>DD</sub>	V	3,4
Termination Reference Voltage	V <sub>TT</sub>	-0.483 x V <sub>DDQ</sub>	0.5 x V <sub>DDQ</sub>	+0.517 x V <sub>DDQ</sub>	V	5

- Notes:
- Under all conditions V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
  - V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.
  - The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/- 1% V<sub>DD</sub>.
  - For reference: approximate V<sub>DD</sub>/2 +/- 15mV.
  - V<sub>TT</sub> termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

## Operating Temperature Condition

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T <sub>OPER</sub>	0 - 95	°C	1,2

- Notes:
- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD5-2
  - At 0 - 85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < T<sub>OPER</sub> <= 95°C



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## Input DC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
<b>Command and Address</b>				
Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHCA(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILCA(DC)	VSS	VREF - 0.100	V
<b>DQ and DM</b>				
Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHDQ(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILDQ(DC)	VSS	VREF - 0.100	V

## Input AC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
<b>Command and Address</b>				
AC Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHCA(AC)	VREF + 0.175	-	V
AC Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILCA(AC)	-	VREF - 0.175	V
<b>DQ and DM</b>				
AC Input High (Logic 1) Voltage DDR3-800/1066	VIHDQ(AC)	VREF + 0.175	-	V
AC Input Low (Logic 0) Voltage DDR3-800/1066	VILDQ(AC)	-	VREF - 0.175	V
AC Input High (Logic 1) Voltage DDR3-1333	VIHDQ(AC)	VREF + 0.150	-	V
AC Input Low (Logic 0) Voltage DDR3-1333	VILDQ(AC)	-	VREF - 0.150	V

## Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	DDR3-800/1066		DDR3-1333		Unit
		Min	Max	Min	Max	
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	5.5	6.5	5.5	6.5	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	5.5	6.5	5.5	6.5	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	7	10/9.4	7	9	pF



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## IDD Specification

Condition	Symbol	DDR3-1066		DDR3-800	Unit
		-K9	-F8	-E7	
<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS MIN(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	1180	1090	1000	mA
<b>Operating one bank active-read-precharge current;</b> IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS MIN(IDD)}$ ; $t_{RCD} = t_{RCD(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	1360	1270	1180	mA
<b>Precharge power-down current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F**	640	550	550	mA
	IDD2P-S**	280	280	280	mA
<b>Precharge standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N**	1180	1090	1000	mA
<b>Precharge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	1090	1000	910	mA
<b>Active power-down current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	730	640	550	mA
<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; $t_{RAS} = t_{RAS MAX(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	1180	1090	1000	mA
<b>Operating burst read current;</b> All banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1990	1630	1360	mA
<b>Operating burst write current;</b> All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	1900	1630	1360	mA
<b>Burst refresh current;</b> $t_{CK} = t_{CK(IDD)}$ ; Refresh command at every $t_{RFC(IDD)}$ interval; CE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	4420	4060	3700	mA
<b>Self refresh current;</b> CK and CK# at 0V; $CKE \leq 0.2V$ ; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	126	126	126	mA
<b>Extended Temperature Range Self refresh current;</b> CK and CK# at 0V; $CKE \leq 0.2V$ ; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6 = 0 and A7 = 1	IDD6ET**	162	162	162	mA
<b>Operating bank interleave read current;</b> All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 \cdot t_{CK(IDD)}$ ; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RRD} = t_{RRD(IDD)}$ ; $t_{RCD} = 1 \cdot t_{CK(IDD)}$ ; CE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	4600	3700	3340	mA

Notes: IDD specification is based on Micron 1Gb F-die components.  
 \*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P ( CKE LOW) mode.  
 \*\*: Value calculated reflects all module ranks in this operating condition.



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AC TIMING PARAMETERS & SPECIFICATIONS									
Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit	
		MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock Timing</b>									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	
Average Clock Period	tCK(avg)	1.5	<1.875	1.875	<2.5	2.5	3.3	ns	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter (Period)	tJIT(per)	-80	80	-90	90	-100	100	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	-80	80	-90	90	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	160		180		200		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140		160		180		ps	
Cumulative error across 2 cycles	tERR(2per)	-118	118	-132	132	-147	147	ps	
Cumulative error across 3 cycles	tERR(3per)	-140	140	-157	157	-175	175	ps	
Cumulative error across 4 cycles	tERR(4per)	-155	155	-175	175	-194	194	ps	
Cumulative error across 5 cycles	tERR(5per)	-168	168	-188	188	-209	209	ps	
Cumulative error across 6 cycles	tERR(6per)	-177	177	-200	200	-222	222	ps	
Cumulative error across 7 cycles	tERR(7per)	-186	186	-209	209	-232	232	ps	
Cumulative error across 8 cycles	tERR(8per)	-193	193	-217	217	-241	241	ps	
Cumulative error across 9 cycles	tERR(9per)	-200	200	-224	224	-249	249	ps	
Cumulative error across 10 cycles	tERR(10per)	-205	205	-231	231	-257	257	ps	
Cumulative error across 11 cycles	tERR(11per)	-210	210	-237	237	-263	263	ps	
Cumulative error across 12 cycles	tERR(12per)	-215	215	-242	242	-269	269	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	$tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min$ $tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max$							
Absolute clock HIGH pulse width	tCH(abs)	0.43		0.43		0.43		tCK(avg)	
Absolute clock Low pulse width	tCL(abs)	0.43		0.43		0.43		tCK(avg)	
<b>Data Timing</b>									
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	125	-	150	-	200	ps	
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	
DQ low-impedance time from CK, CK	tLZ(DQ)	-500	250	-600	300	-800	400	ps	
DQ high-impedance time from CK, CK	tHZ(DQ)	-	250	-	300	-	400	ps	
Data setup time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	-10	-	25	-	75	-	ps	
Data hold time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	65	-	100	-	150	-	ps	



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AC TIMING PARAMETERS & SPECIFICATIONS								
Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
<b>Data Strobe Timing</b>								
DQS, DQS READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS output high time	tQSH	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS output low time	tQSL	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-255	255	-300	300	-400	400	ps
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	-600	300	-800	400	ps
DQS, DQS high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	250	-	300	-	400	ps
DQS, DQS differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DQS, DQS differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)
<b>Command and Address Timing</b>								
DLL locking time	tDLLK	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	tCK(avg)
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	max (12tCK,15ns)	-	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)			WR + roundup (tRP / tCK(AVG))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	37.5	70,000	37.5	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	max (4tCK,10ns)	-	
Four activate window for 1KB page size	tFAW	30	-	37.5	-	40	-	ns
Four activate window for 2KB page size	tFAW	45	-	50	-	50	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	125	-	200	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	200	-	275	-	ps



# Product Specifications

PART NO:

VL33B5663F-K9M-F8M-E7M

REV: 1.1

## AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
<b>Refresh Timing</b>								
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	110	-	110	-	110	-	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8		7.8		7.8		us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9		3.9		3.9		us
<b>Calibration Timing</b>								
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	tCK
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	tCK
<b>Reset Timing</b>								
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	
<b>Self Refresh Timing</b>								
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
<b>Power Down Timing</b>								
Exit Power Down with DLL to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3tCK, 6ns)	-	max(3tCK, 7.5ns)	-	max(3tCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	max(10tCK, 24ns)	-	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5.625ns)	-	max(3tCK, 5.625ns)	-	max(3tCK, 7.5ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK



# Product Specifications

PART NO: VL33B5663F-K9M-F8M-E7M

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## AC TIMING PARAMETERS & SPECIFICATIONS

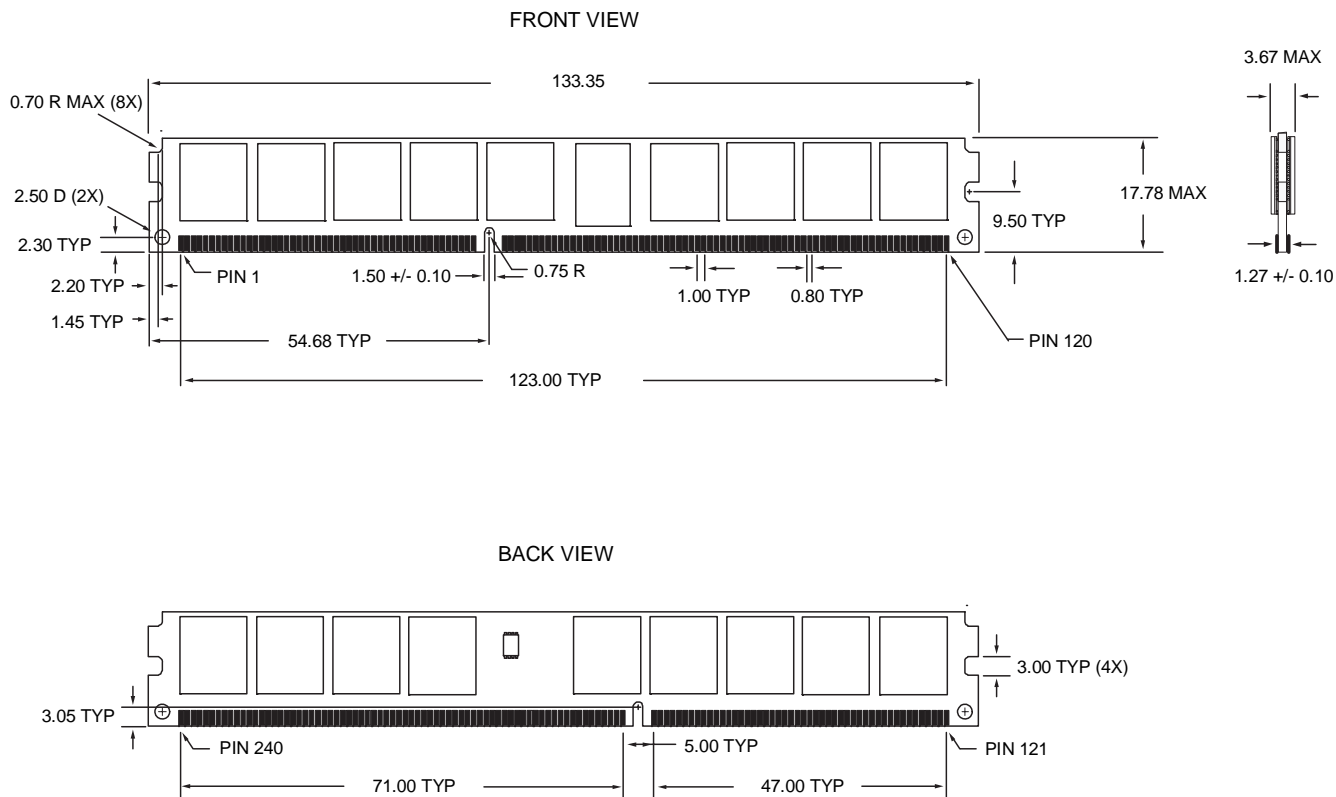
Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	WL + 4 +(tWR/tCK)	-	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	WL + 4 +WR + 1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/tCK)	-	WL + 2 +(tWR/tCK)	-	WL + 2 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	WL + 2 +WR + 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tCK
<b>ODT Timing</b>								
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOPFD	1	9	1	9	1	9	ns
ODT turn-on	tAON	-250	250	-300	300	-400	400	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
<b>Write Leveling Timing</b>								
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK
DQS/DQS delay after tDQSS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	245	-	325	-	ps
Hold time for tDQSS latch	tWLH	195	-	245	-	325	-	ps
Write leveling output delay	tWLO	0	9	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns

# Product Specifications

PART NO: **VL33B5663F-K9M-F8M-E7M**

REV: **1.1**

## Package Dimensions



Note: All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.



# Product Specifications

PART NO: VL33B5663F-K9M-F8M-E7M

REV: 1.1

## Revision History

Date	Rev.	Page	Changes
11/10/08	1.0	All	Release spec
09/01/09	1.1	1, 4, 6,~11	Feature upadate page 1 Operating temperature update page 4 IDD table update page 6 Timing update page 7~10 Package dimension update page 11