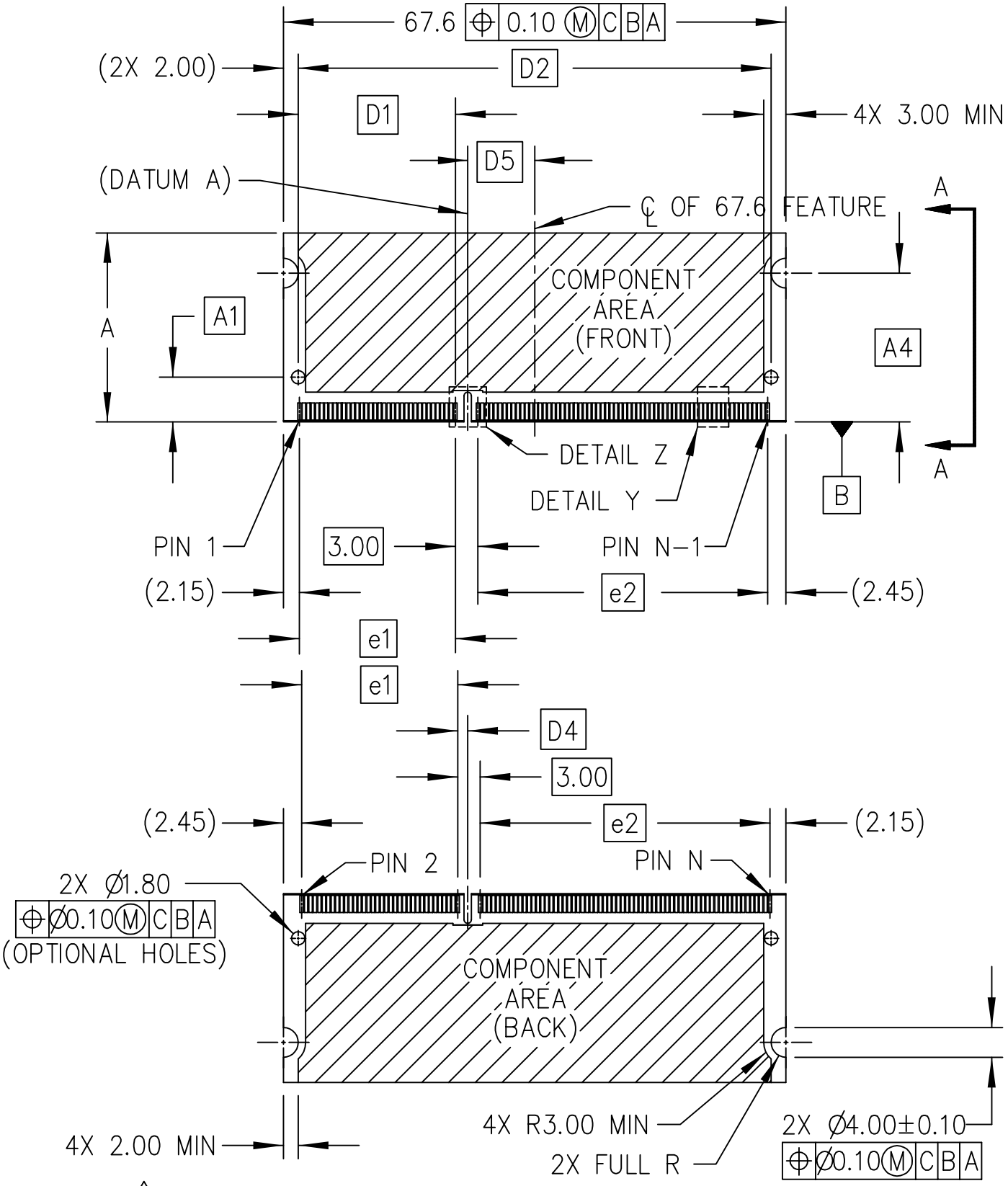
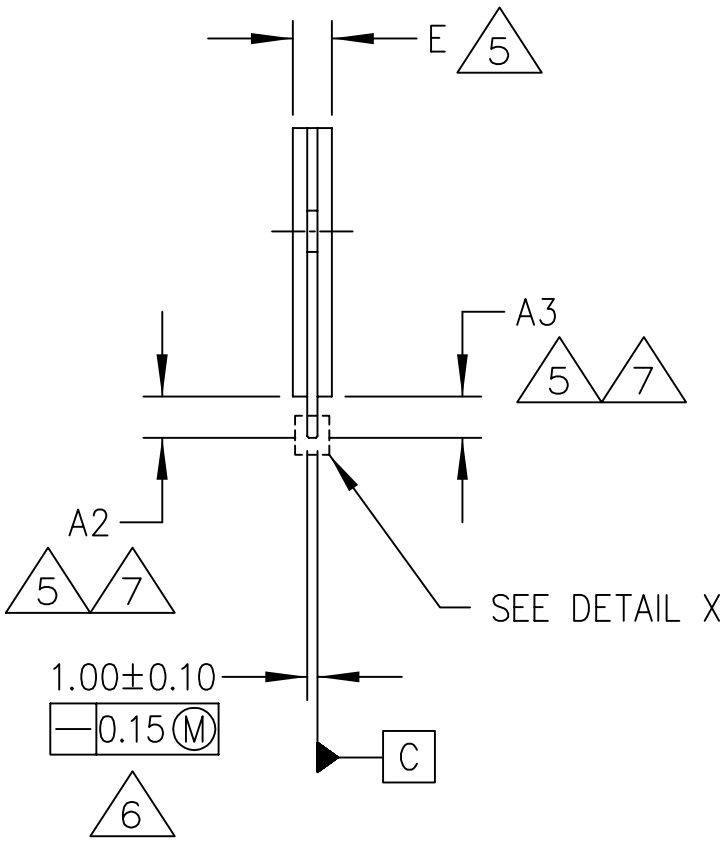


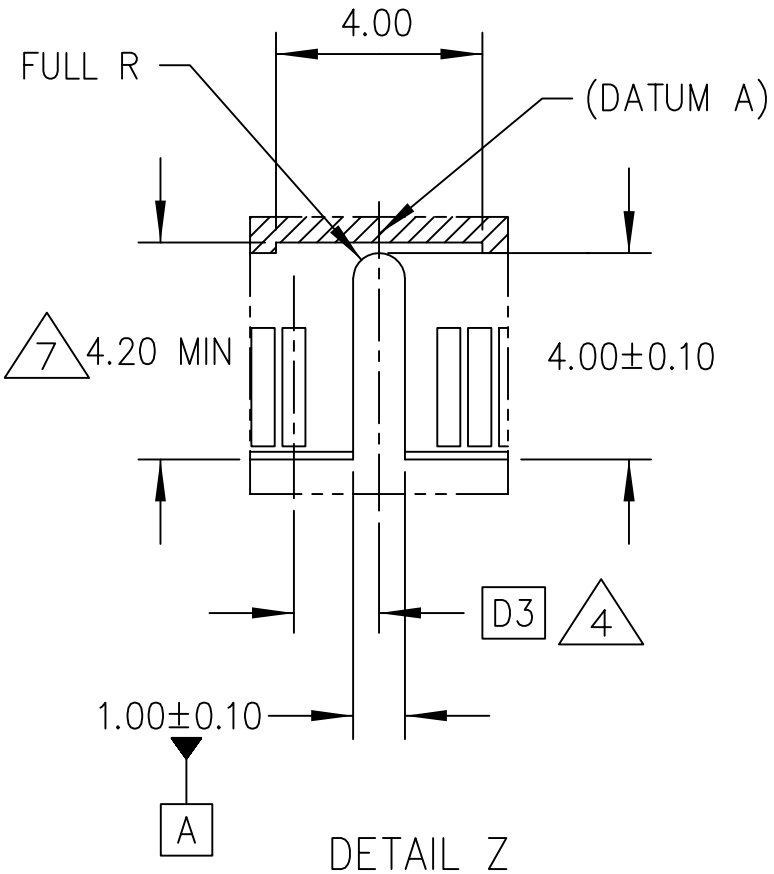
PATENT ISSUES 10

JEDEC SOLID STATE PRODUCT OUTLINE	THIS REGISTERED OUTLINE HAS BEEN PREPARED AND PUBLISHED BY THE JEDEC JC–11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USE IN THE ELECTRONICS INDUSTRY. CHANGES ARE LIKELY TO OCCUR.

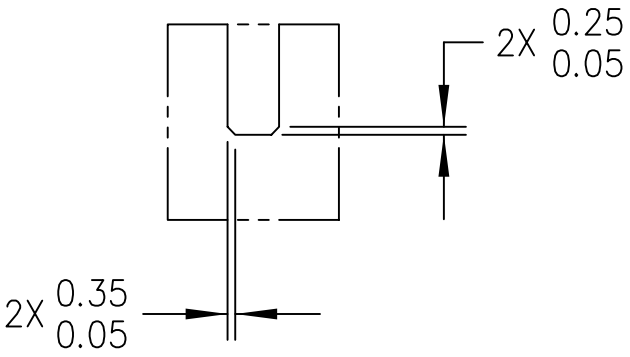
TITLE:	PACKAGE DESIGNATOR:	ISSUE:	DATE:		PAGE:
204 PIN DDR3 SODIMM, 0.60 LEAD CENTERS		C	08/08	MO–268	1 OF 9



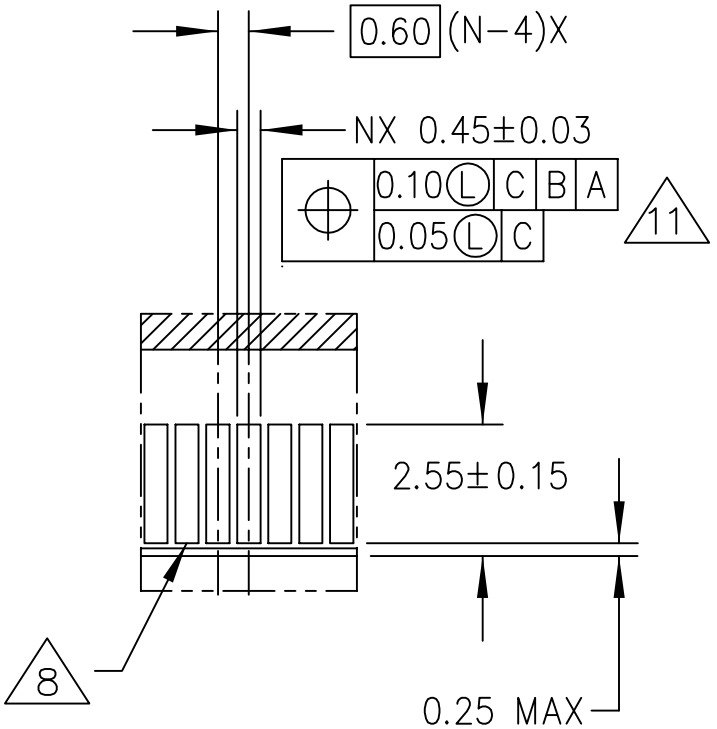
VIEW A–A



DETAIL Z



DETAIL X
(OPTIONAL)
9



DETAIL Y

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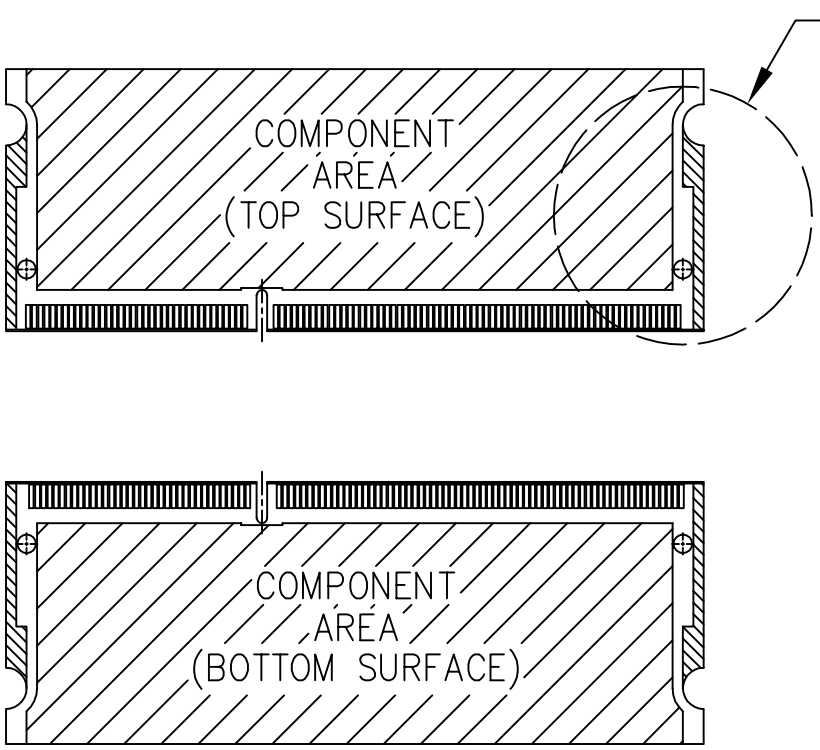
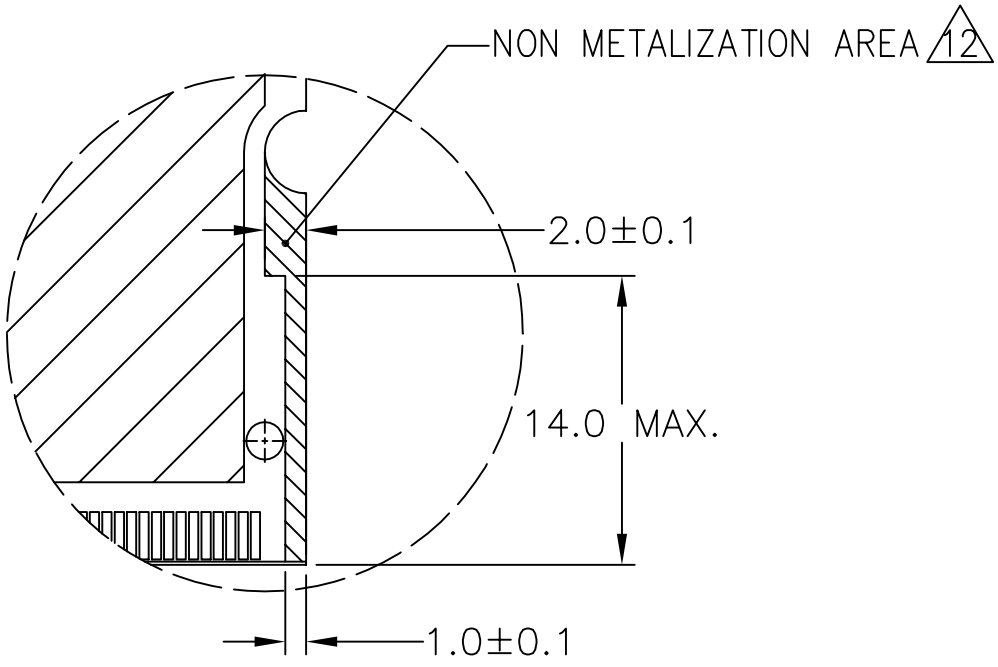
COMMON DIMENSION TABLE				
SYMBOL	MIN	NOM	MAX	NOTES
A1	6.00 BASIC			
A2	4.00	--	--	5, 7
A3	4.00	--	--	5, 7
A4	20.00 BASIC			
D1	21.15 BASIC			
D2	63.60 BASIC			
E	--	--	3.80	5
e1	21.00 BASIC			
e2	39.00 BASIC			
N	204			
D3	1.65 BASIC			4
D4	1.35 BASIC			
D5	9.00 BASIC			
ISSUE	A			
REF	14-085			
NOTES	1,2,3			

SDRAM VARIATIONS			
"A" DIMENSION	AA	BA	CA
MIN	25.25	31.60	29.85
NOMINAL	25.40	31.75	30.00
MAX	25.55	31.90	30.15
ISSUE	A		
REF	14-085		
NOTES	1,2,3		

NON-METALIZATION DEFINITION OUTER LAYERS





DETAIL W (4 PLACES)

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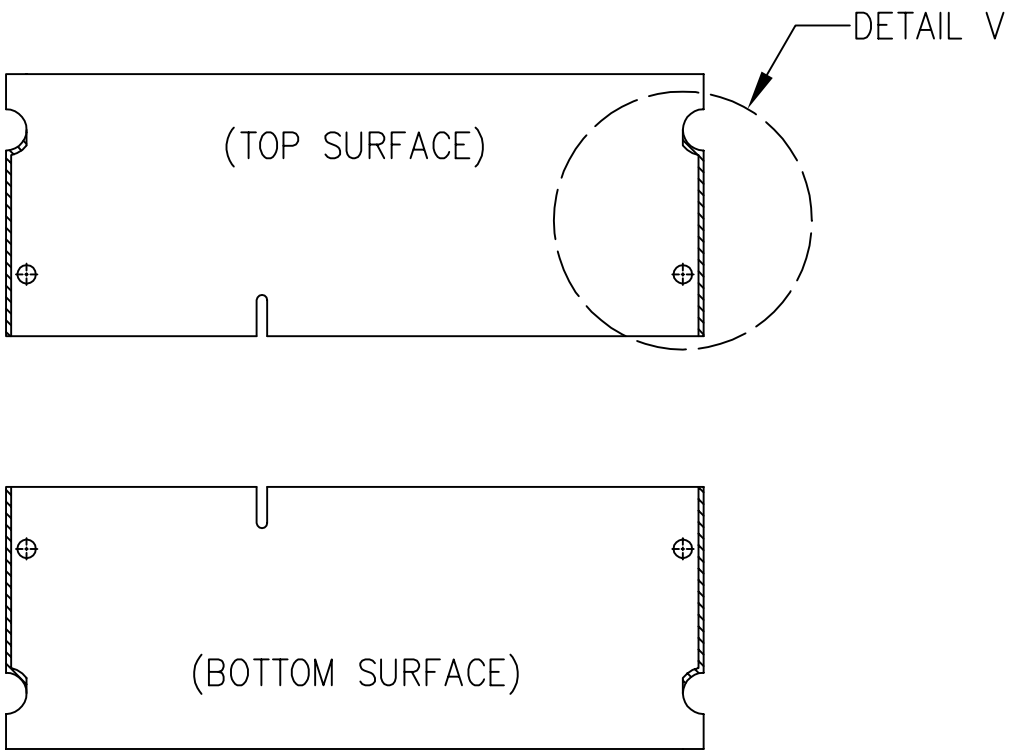
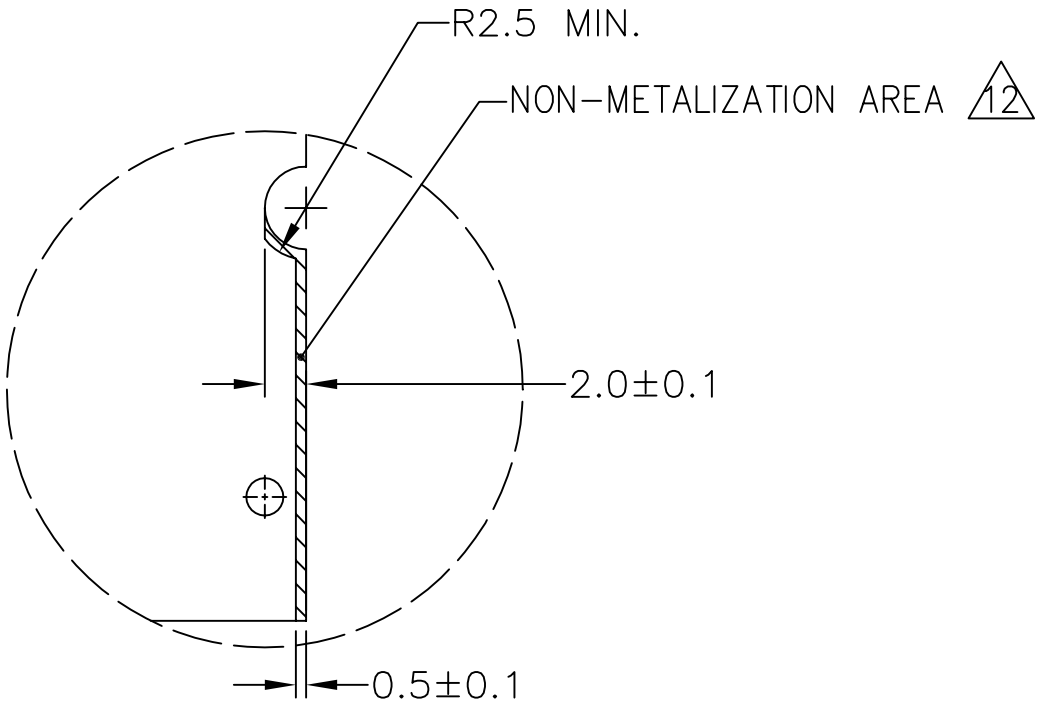
NON-METALIZATION DEFINITION ALL INNER LAYERS





DETAIL V (4 PLACES)

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.

2. TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. ALL DIMENSIONS ARE MM.

4 THE POSITION OF THE NOTCH IDENTIFIES THE OPERATIONAL VOLTAGE: 1.5 VOLTS.
THE JC–45.3 COMMITTEE CONTROLS THIS INFORMATION.
IT IS SHOWN HERE FOR REFERENCE ONLY, AND SUBJECT TO CHANGE.

5 DIMENSIONS APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES.
PCB THICKNESS NOT TO BE EXCEEDED OUTSIDE OF COMPONENT AREA.

6 CARD THICKNESS APPLIES ACCROSS TABS AND INCLUDES
PLATING AND/OR METALIZATION.

7 BORDER OF COMPONENT AREA.

8 EDGE OF CONTACT PADS SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

9 THE ADDITION OF THIS BEVEL IS A FABRICATION OPTION AND IS NOT REQUIRED.
THE BEVEL AIDS THE INSERTION OF THE MODULES INTO THE CONNECTOR.
THE BEVEL IS NOT TO HIT THE PLATED CONTACTS.

10 PATENT CLAIM:
US PATENT NO. 5,227,664 MAY BE RELATED TO CERTAIN IMPLEMENTATIONS
OF THIS PACKAGE OUTLINE.

11 APPLICATION NOTE:
RECOMMENDED PLATING FOR CONTACT PADS ARE:
1) PREFERABLE PLATING: ELECTROLYTIC GOLD PLATING 0.76 MICROMETERS MINIMUM OVER ELECTROLYTIC Ni 2.00 MICROMETERS MINIMUM.
2) ALTERNATIVE PLATING: GOLD PLATING 0.05 – 0.75 MICROMETERS OVER Ni 2.00 MICROMETERS MINIMUM MUST USE AN ELECTRONIC CONTACT GRADE CORROSIVE BARRIER LUBRICANT.

12 'METALIZATION' IS DEFINED AS ANY METAL SURFACE THAT HAS A RETURN PATH TO POWER SUPPLY OR GROUND, THROUGH A COMPONENT OR CONDUCTIVE PLANE VCC OR VDD, BLIND OR PLATED THROUGH HOLE (PTH), AS WELL AS NARROW OR WIDE TRACES. ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDER CODE, ETC. THAT DO NOT HAVE A METALS AS A RETURN PATH ARE ACCEPTABLE.

'NON-METALIZATION' IS DEFINED AS THE OPPOSITE TO 'METALIZATION' AND DOES NOT INCLUDE ANY METAL OR CONDUCTIVE ELEMENTS THAT MAY CAUSE ELECTRICAL SHORT CIRCUIT.

HOWEVER, ANY SURFACE METALS SUCH AS CONNECTOR PIN IDENTIFICATION, PCB VENDOR NAME OR CODE, ETC. THAT DOES NOT HAVE CONDUCTIVE RETURN PATH TO VCC OR VDD IS ACCEPTABLE.

Change Record

If the changes involves any words added or deleted (excluding deletion of accidentally repeated words), the change is included. Punctuation chages may or may not be included.

Initial Issue: A	Date: Jan 2006	Item: 14–085

Revision History:

Issue: B	Date: Nov 06	Item: 11.14–106E

Location	Change from:	Change to:
Page 1	PIN N/2	PIN N–1

Issue: C	Date: July 08	Item: 11.14–117

Location	Change from:	Change to:
Page 1 THREE OF TOLERANCE BOX	⌖ | 0.10 Ⓜ | C | A | B	⌖ | 0.10 Ⓜ | C | B | A
Page 1	℄ OF D	℄ OF 67.6 FEATURE
Page 1	2X 4.00±0.10	2X Ø4.00±0.10
Page 2 DETAIL Z	4.20	4.20 MIN
Page 2 DETAIL X	2X 0.25 0.05	2X 0.35 0.05
Page 2 DETAIL Y	⌖ | 0.10Ⓛ | C | A | B ⌖ | 0.05Ⓛ | C	⌖ | 0.10Ⓛ | C | B | A 0.05Ⓛ | C
	2.55	2.55± 0.15
Page 1–9 TITLE	204 PIN DDR3 S.O.DIMM,	204 PIN DDR3 SODIMM,

Location	Change from:	Change to:

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: 204 PIN DDR3 SODIMM, 0.60 LEAD CENTERS	ISSUE: C	DATE: 08/08	MO–268	PAGE: 9 OF 9